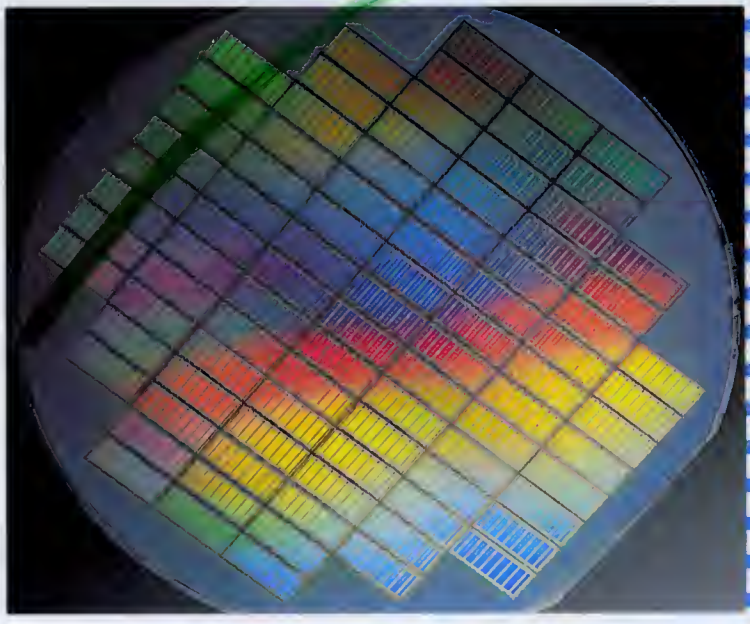
TOSHIBA

Static RAM 1992



DISTRIBUTED BY:

MERIT

MERIT ELECTRONICS, INC.
2070 Ringwood Ave.
San Jose, CA 95131
(408) 434-0800

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA

Static RAM

1992

1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Depertment of Commerce prior to export. Any export or re-export directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.

2. LIFE SUPPORT POLICY

   Toshiba products described in this databook are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

   A critical component is any component of a life support system whose failure to perform mey ceuse e malfunction or failure of the life support system, or may affect its safety or effectiveness.

3. The information in this databook has been carefully checked and is believed to be reliable, however, no responsibility can be assumed for inaccuracies that may not have been caught. All information in this databook is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.

TABLE OF CONTENTS
STATIC RAM PRODUCT GUIDE
CROSS REFERENCE
PART NUMBER GUIDE

CMOS PSEUDO STATIC RAM

CMOS STANDARD STATIC RAM

CMOS HIGH SPEED STATIC RAM

BiCMOS HIGH SPEED STATIC RAM

TABLE OF CONTENTS

	DESCRIPTION	ISSUE DATE	PAGE
CMOS Pseudo Static RAM			
TC51832P/SP/F/PL/SPL/FL	32Kx8	11-88	A-1
TC518128AP/ASP/AF/AFW/APL/ASPL/ AFL/AFWL/AFTL/ATRL	128Kx8, CE1 AND CE2	10-91	A-13
TC518128APL/AFL/AFWL/AFTL/ATRL-LV	128Kx8, CE1 AND CE2, LOW VOLTAGE	1-92	A-28
TC518129AP/ASP/AF/AFW/APL/ASPL/ AFL/AFWL/AFTL/ATRL	128Kx8, CE AND CS	10-91	A-48
TC518129APL/AFL/AFWL/AFTL/ATRL-LV	128Kx8, CE AND CS, LOW VOLTAGE	1-92	A-64
TC518512PL/FL/FTL/TRL	512Kx8, CE AND OE	12-91	A-84
CMOS Static RAM			
TC55257BPL/BFL/BSPL/BFTL/BTRL	32Kx8	4-91	B-1
TC55257BPL/BFL/BSPL/BFTL/BTRL-L	32Kx8, LOW POWER	4-91	B-13
TC55257BPI/BFI/BSPI-L	32Kx8, INDUSTRIAL TEMP, LOW POWER	4-91	B-25
TC551001PL/FL	128Kx8	10-91	B-35
TC551001PL/FL-L	128Kx8, LOW POWER	10-91	B-45
TC551001PI/FI-L	128Kx8, INDUSTRIAL TEMP, LOW POWER	10-91	B-55
TC551001APL/AFL/AFTL/ATRL	128Kx8	10-91	B-65
TC551001APL/AFL/AFTL/ATRL-L	128Kx8, LOW POWER	10-91	B-77
TC551001API/AFI/AFTI/ATRI	128Kx8, INDUSTRIAL TEMP	10-91	B-89
TC551001API/AFI/AFTI/ATRI-L	128Kx8, INDUSTRIAL TEMP, LOW POWER	10-91	B-101
CMOS High Speed Static RAM			
TC5588P/J	8Kx8	2-91	C-1
TC5589P/J	8Kx9	2-91	C-9
TC55416P-H	16Kx4	2-91	C-17
TC55417P/J-H	16Kx4, WITH OE	2-91	C-23
TC55187T	8Kx18/4Kx18x2, A12 & CE ASYNCHRONOUS	10-90	C-31
TC55188T	8Kx18/4Kx18x2	1-91	C-49
TC55464P/J	64Kx4	1-91	C-65
TC55465P/J	64Kx4, WITH OE	1-91	C-73
TC55328P/J	32Kx8	1-91	C-81
TC55329P/J	32Kx9	5-90	C-89
TC551632J	32Kx16	10-91	C-97
TC551664J	84Kx16, UPPER/LOWER BYTE CONTROL	11-91	C-105
BiCMOS High Speed Static RAM			
TC55B88P/J	8Kx8	3-91	D-1
TC55B417P/J	16Kx4, WITH OE	3-91	D-9
TC55B484P/J	64Kx4	8-91	D-17
TC55B465P/J	64Kx4, WITH OE	8-91	D-27
TC55B328P/J	32Kx8	8-91	D-37
TC55B329P/J	32Kx9	8-91	D-47
TC55B4256P/J	256Kx4	10-91	D-57
TC55B4257P/J	256Kx4, WITH OE	10-91	D-65
TC55B8128P/J	128Kx8, WITH OE	10-91	D-73

Static RAM Product Guide

1. CMOS Pseudo Static RAM

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION Max (mW)		PIN COUNT	PACKAGE						PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		P	SP	F	FW	FT	TR	
256K Bit	TC51832P/SP/F-85	32Kx8	85	35	5V±10%	303	5.5	28	■	■	■				0.600 (P) 0.300 (SP) 0.450 (F)
	TP51832P/SP/F-10		100	40		248			■	■	■				
	TC51832P/SP/F-12		120	50		220			■	■	■				
	TC51832PL/SPL/FL-85		85	35		303	0.55		■	■	■				
	TC51832PL/SPL/FL-10		100	40		248			■	■	■				
	TC51832PL/SPL/FL-12		120	50		220			■	■	■				
1M Bit	TC518128AP/ASP/AF/AFW-80	128Kx8 (CE1, CE2)	80	35		385	5.5	32	■	■	■	■			0.600 (P) 0.300 (SP) 0.450 (F) 0.525 (FW) 8x20mm FT(I), TR(I)
	TC518128AP/ASP/AF/AFW-10		100	40		330			■	■	■	■			
	TC518128AP/ASP/AF/AFW-12		120	50		275			■	■	■	■			
	TC518128APL/ASPL/AFL/AFWL-80		80	35		385	1.1		■	■	■	■			
	TC518128APL/ASPL/AFL/AFWL-10		100	40		330			■	■	■	■			
	TC518128APL/ASPL/AFL/AFWL-12		120	50		275			■	■	■	■			
	TC518128AFTL/ATRL-80		80	35		385	1.1						■	■	
	TC518128AFTL/ATRL-10		100	40		330							■	■	
	TC518128AFTL/ATRL-12		120	50		275							■	■	
	TC518128APL/AFL/AFWL-80LV		80	35		385	0.3 (3V)*		■		■	■			
	TC518128APL/AFL/AFWL-10LV		100	40		330			■		■	■			
	TC518128APL/AFL/AFWL-12LV		120	50		275			■		■	■			
	TC518128AFTL/ATRL-80LV		80	35		385	0.3 (3V)*					■	■		
	TC518128AFTL/ATRL-10LV		100	40		330						■	■		
	TC518128AFTL/ATRL-12LV		120	50		275						■	■		
	TC518128AXXX-LV (3.3V)		200	80	3.3V±5%	69.3	0.3465		■		■	■	■	■	
	TC518129AP/ASP/AF/AFW-80	128Kx8 (CE, CS)	80	35	5V±10%	385	5.5		■	■	■	■			
	TC518129AP/ASP/AF/AFW-10		100	40		330			■	■	■	■			
	TC518129AP/ASP/AF/AFW-12		120	50		275			■	■	■	■			
	TC518129APL/ASPL/AFL/AFWL-80		80	35		385	1.1		■	■	■	■			
	TC518129APL/ASPL/AFL/AFWL-10		100	40		330			■	■	■	■			
	TC518129APL/ASPL/AFL/AFWL-12		120	50		275			■	■	■	■			
	TC518129AFTL/ATRL-80		80	35		385	1.1						■	■	
	TC518129AFTL/ATRL-10		100	40		330							■	■	
	TC518129AFTL/ATRL-12		120	50		275							■	■	
	TC518129APL/AFL/AFWL-80LV		80	35		385	0.3 (3V)*		■		■	■			
	TC518129APL/AFL/AFWL-10LV		100	40		330			■		■	■			
	TC518129APL/AFL/AFWL-12LV		120	50		275			■		■	■			
	TC518129AFTL/ATRL-80		80	35		385	0.3 (3V)*						■	■	
	TC518129AFTL/ATRL-10		100	40		330							■	■	
	TC518129AFTL/ATRL-12		120	50		275							■	■	
	TC518129AXXX-LV (3.3V)		200	80	3.3V±5%	69.3	0.3465		■		■	■	■	■	
4M Bit	TC518512PL/FL/FTL/TRL-70	512Kx8	70	30	5V±10%	385	1.1	32	■		■		■	■	0.600 (P) 0.525 (F) 0.400FT (I) 0.400TR (I)
	TC518512PL/FL/FTL/TRL-80		80	30		330			■		■		■	■	
	TC518512PL/FL/FTL/TRL-10		100	40		275			■		■		■	■	

P = PLASTIC DIP, SP = PLASTIC SKINNY DIP, F = PLASTIC FLAT PACKAGE(SOP) , FW = PLASTIC FLAT WIDE PACKAGE(SOP)
FT = THIN SMALL OUTLINE PACKAGE (TSOP), TR = REVERSE TYPE TSOP
* IN SELF REFRESH MODE WITH DATA RETENTION SUPPLY VOLTAGE OF 3V

2. CMOS Static RAM

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max (ns)	OUTPUT ENABLE ACCESS TIME Max (ns)	POWER SUPPLY (V)	POWER DISSIPATION Max (mW) ACTIVE	POWER DISSIPATION Max (mW) STANDBY	PIN COUNT	PACKAGE P	PACKAGE SP	PACKAGE F	PACKAGE FT	PACKAGE TR	PACKAGE WIDTH (inch)
256K Bit	TC55257BPL/BFL/BSPL-85	32Kx8	85	45	5V±10%	330	0.550	28	■	■	■			0.600 (P) 0.300 (SP) 0.450 (F) FT (I) TR (I)
	TC55257BFTL/BTRL-85		85	45								■	■	
	TC55257BPL/BFL/BSPL-10		100	50					■	■	■			
	TC55257BFTL/BTRL-10		100	50								■	■	
	TC55257BPL/BFL/BSPL-85L		85	45			0.185		■	■	■			
	TC55257BFTL/BTRL-85L		85	45								■	■	
	TC55257BPL/BFL/BSPL-10L		100	50					■	■	■			
	TC55257BFTL/BTRL-10L		100	50								■	■	
	TC55257BPI/BFI/BSPI-10L		100	50			0.275		■	■	■			
1M Bit	TC551001PL/FL-85	128Kx8	85	45	5V±10%	385	0.550	32	■		■			0.600 (P) 0.525 (F) 8 x 20mm FT(I), TR(I)
	TC551001PL/FL-10		100	50					■		■			
	TC551001PL/FL-85L		85	45			0.165		■		■			
	TC551001PL/FL-10L		10	50					■		■			
	TC551001PI/FI-10L		10	50			0.385		■		■			
	TC551001APL/AFL/AFTL/ATRL-70		70	35		330	0.55		■		■	■	■	
	TC551001APL/AFL/AFTL/ATRL-85		85	45					■		■	■	■	
	TC551001APL/AFL/AFTL/ATRL-10		10	50					■		■	■	■	
	TC551001APL/AFL/AFTL/ATRL-70L		70	35			0.165		■		■	■	■	
	TC551001APL/AFL/AFTL/ATRL-85L		85	45					■		■	■	■	
	TC551001APL/AFL/AFTL/ATRL-10L		10	50					■		■	■	■	
	TC551001API/AFI/AFTI/ATRI-10		10	50			1.1		■		■	■	■	
	TC551001API/AFI/AFTI/ATRI-10L		10	50			0.385		■		■	■	■	

P = PLASTIC DIP, SP = PLASTIC SKINNY DIP, F = PLASTIC FLAT PACKAGE(SOP) FT = THIN SMALL OUTLINE PACKAGE (TSOP)
TR = REVERSE TYPE TSOP

3. CMOS High Speed Static RAM (I)

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max (ns)	OUTPUT ENABLE ACCESS TIME Max (ns)	POWER SUPPLY (V)	POWER DISSIPATION MAX (mW) ACTIVE	POWER DISSIPATION MAX (mW) STANDBY	PIN COUNT	PACKAGE P	PACKAGE J	PACKAGE WIDTH (inch)
64K	TC55416P-15H	16Kx4	15		5V±10%	660	5.5	22	■		0.300
	TC55416P-20H		20			550			■		
	TC55416P-25H		25						■		
	TC55418P-35H		35			440			■		
	TC55417P/J-15H		15	9		660		24	■	■	
	TC55417P/J-20H		20	10		550			■	■	
	TC55417P/J-25H		25	10					■	■	
	TC55417P/J-35H		35	10		440			■	■	
	TC5568P/J-15	8Kx8	15	9		743		28	■	■	
	TC5568P/J-20		20	10		633			■	■	
	TC5568P/J-25		25	12					■	■	
	TC5568P/J-35		35	12					■	■	
72K	TC5589P/J-15	8Kx9	15	9	5V±10%	743	5.5	28	■	■	
	TC5589P/J-20		20	10		633			■	■	
	TC5589P/J-25		25	12					■	■	
	TC5589P/J-35		35	12					■	■	
256K	TC55328P/J-17	32Kx8	17	9	5V±5%	735	5.5	28	■	■	
	TC55328P/J-20		20	10	5V±10%	770			■	■	
	TC55328P/J-25		25	12					■	■	
	TC55328P/J-35		35	15		660			■	■	
	TC55464P/J-17	64Kx4	17		5V±5%	630		24	■	■	
	TC55464P/J-20		20		5V±10%	660			■	■	
	TC55464P/J-25		25						■	■	
	TC55464P/J-35		35			550			■	■	
	TC55465P/J-17		17	9	5V±5%	630		28	■	■	
	TC55465P/J-20		20	10	5V±10%	660			■	■	
	TC55465P/J-25		25	12					■	■	
	TC55465P/J-35		35	15		550			■	■	
288K	TC55329P/J-17	32Kx9	17	9	5V±5%	735	5.5	32	■	■	
	TC55329P/J-20		20	10	5V±10%	770			■	■	
	TC55329P/J-25		25	12					■	■	
	TC55329P/J-35		35	15		660			■	■	
512K	TC551632J-20	32Kx16	20	10	5V±10%	1210	5.5	40		■	0.400
	TC551632J-25		25	12		1100				■	
	TC551632J-35		35	17		935				■	
1M	TC551664J-15	64Kx18	15	8	5V±10%	1430	5.5	44		■	
	TC551664J-20		20	10		1210				■	
	TC551664J-25		25	12		1100				■	

P = PLASTIC DIP, J = PLASTIC SOJ

3. CMOS High Speed Static RAM (II)

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION Max(mW) ACTIVE	POWER DISSIPATION Max(mW) STANDBY	PIN COUNT	PACKAGE P J PLCC	PACKAGE WIDTH (inch)
144K	TC55187T-20	8Kx18 / 4Kx18 X2 Way	20	10	5V±10%	1265	220	52	■	0.8
	TC55187T-25		25	10		1210			■	
	TC55187T-30		30	12		1100			■	
	TC55188T-20		20	10		1265			■	
	TC55188T-25		25	10		1210			■	
	TC55188T-30		30	12		1100			■	

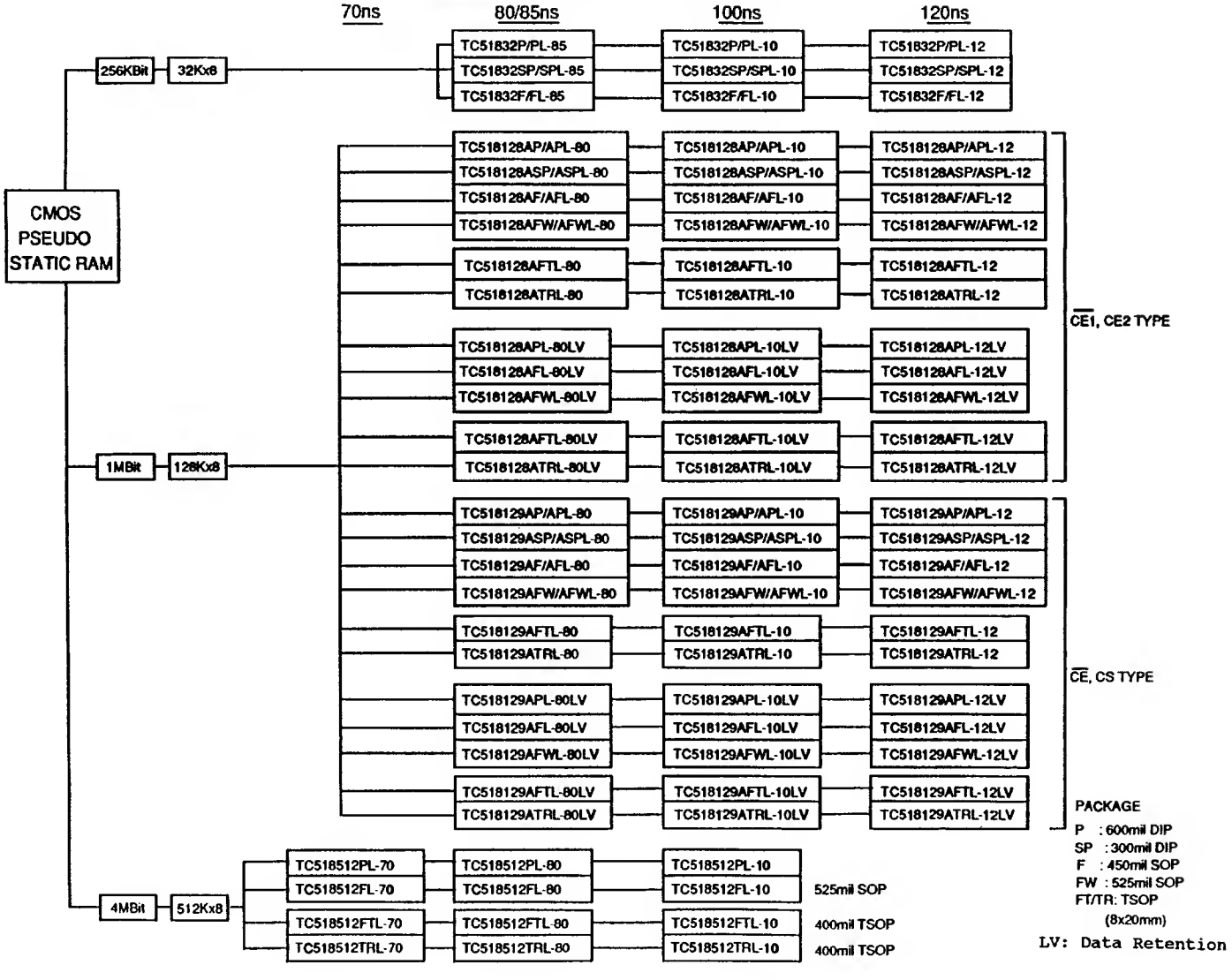
T = PLASTIC LEADED CHIP CARRIER(PLCC)

4. BiCMOS High Speed Static RAM

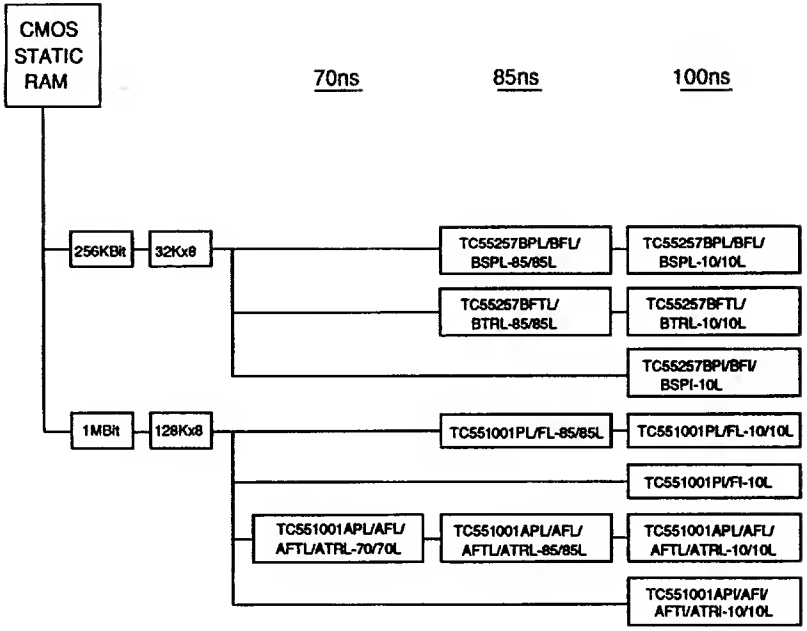
CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION Max(mW)		PIN COUNT	PACKAGE		PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		P	J	
64K	TC55B417P/J-10	16Kx4	10	8	5V±5%	630	55	24	■	■	0.300
	TC55B417P/J-12		12	7	5V±10%	660			■	■	
	TC55B88P/J-10	8Kx8	10	6	5V±5%	813.75		28	■	■	
	TC55B88P/J-12		12	7	5V±10%	852.5			■	■	
256K	TC55B464P/J-10	64Kx4	10		5V±10%	770	82.5	24	■	■	0.300
	TC55B464P/J-12		12						■	■	
	TC55B464P/J-15		15						■	■	
	TC55B465P/J-10		10	5		770	82.5	26	■	■	
	TC55B465P/J-12		12	8					■	■	
	TC55B465P/J-15		15	8					■	■	
	TC55B328P/J-10	32Kx8	10	5		935	82.5		■	■	
	TC55B328P/J-12		12	8					■	■	
	TC55B328P/J-15		15	8					■	■	
288K	TC55B329P/J-10	32Kx9	10	5	5V±10%	935	82.5	32	■	■	
	TC55B329P/J-12		12	6					■	■	
	TC55B329P/J-15		15	8					■	■	
1M	TC55B4256P/J-12	256Kx4	12		5V±10%	715	55	28	■	■	0.400
	TC55B4256P/J-15		15						■	■	
	TC55B4256P/J-20		20						■	■	
	TC55B4257P/J-12	256Kx4	12	7		715	55	32	■	■	
	TC55B2457P/J-15		15	8					■	■	
	TC55B4257P/J-20		20	10					■	■	
	TC55B8128P/J-12	128Kx8	12	7		825	55		■	■	
	TC55B8128P/J-15		15	8					■	■	
	TC55B8128P/J-20		20	10					■	■	

P = PLASTIC DIP, J = PLASTIC SOJ

TOSHIBA PSEUDO STATIC RAM



TOSHIBA CMOS STATIC RAM



F: 450mil SOP

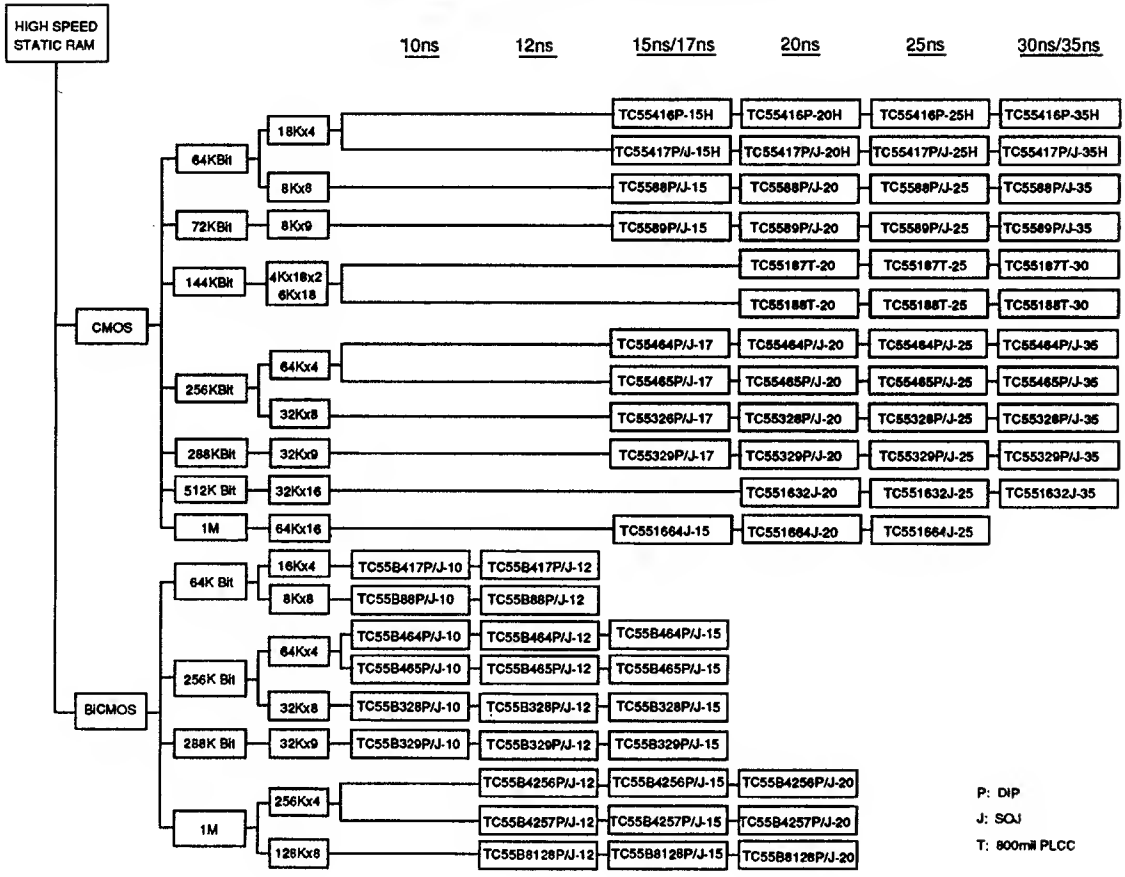
F: 525mil SOP

P: 600mil DIP

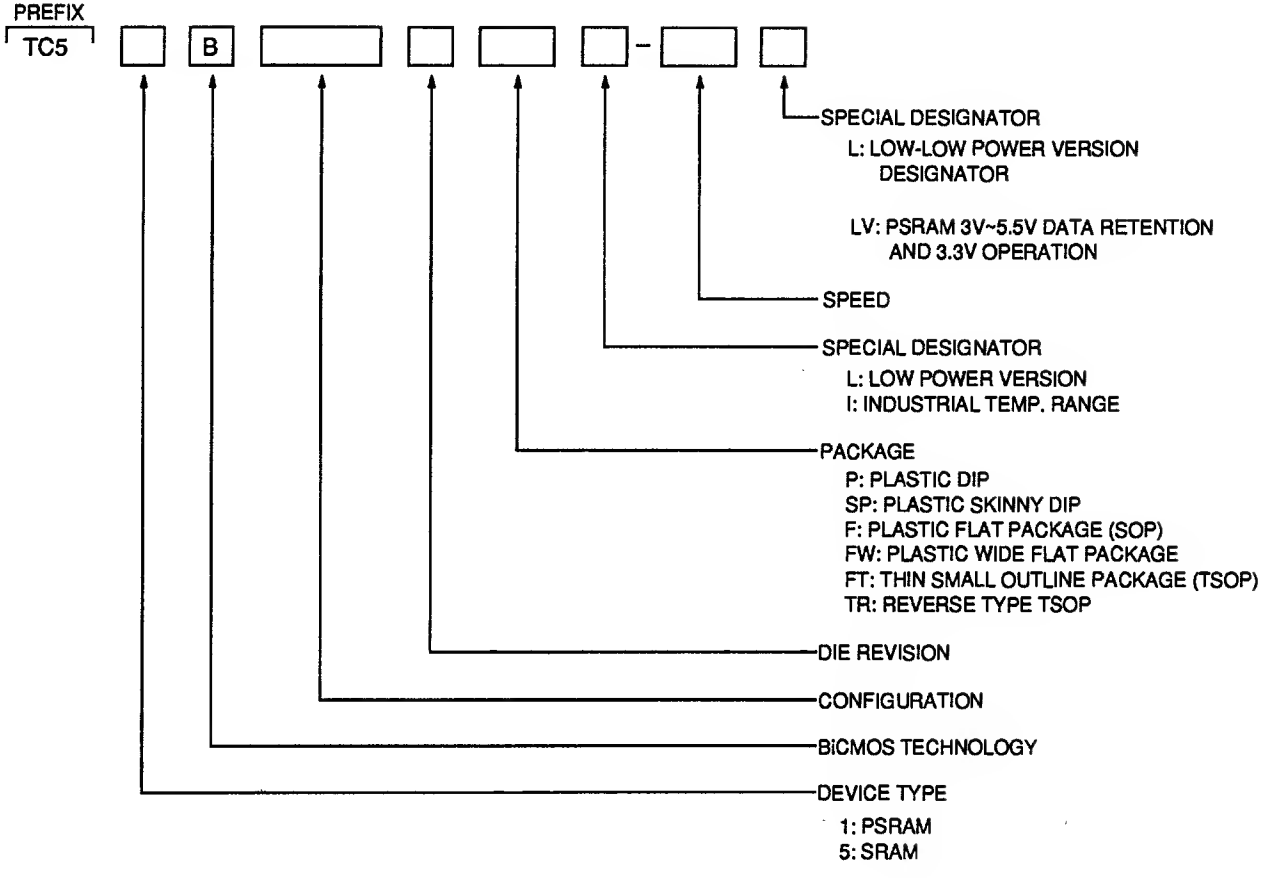
SP: 300mil DIP

FT/TR: TSOP (I)
8x20mm

TOSHIBA HIGH SPEED STATIC RAM



SRAM/PSRAM PART NUMBER GUIDE



Cross Reference

CYPRESS	TOSHIBA	DESCRIPTION	SPEED	CODE
CY7C187A	TC5562	64KX1	15,20,25,(35,45)	HS
CY7C164A	TC55416H	16KX4	(15,20,25,35),45	HS
CY7B164	TC55416H	16KX4	10,12,(15)	HS
CY7C166A	TC55417H	16KX4 OE	(15,20,25,35),45	HS
CY7B166	TC55417H	16KX4 OE	10,12,(15)	HS
CY7B166	TC55B417	16KX4 OE	(10,12),15	HS
CY7C182	TC5589	8KX9	(25,35),45,55	HS
CY7C185A	TC5588	8KX8	(20,25,35),45,55	HS
CY7B185	TC5588	8KX8	10,12,(15)	HS
CY7B185	TC55B88	8KX8	(10,12),15	HS
CY7C194	TC55464	64KX4	(25,35),45	HS
CY7B194	TC55464	64KX4	12,15,(20)	HS
CY7B194	TC55B464	64KX4	(12,15),20	HS
CY7C196	TC55465	64KX4 OE	(25,35),45	HS
CY7B196	TC55465	64KX4 OE	12,15,(20)	HS
CY7B196	TC55B465	64KX4 OE	(12,15),20	HS
CY7C199	TC55328	32KX8	(25,35),45,55	HS
CY7B199	TC55B328	32KX8	(12,15),20	HS
CY7C183	TC55187	4KX18X2	(25),35,45	HS
CY7C184	TC55188	4KX18X2	(25),35,45	HS

FUJITSU	TOSHIBA	DESCRIPTION	SPEED	CODE
MB8464A	TC5565	8KX8	80,(100,150)	STD
MB84256	TC55257	32KX8	70,(100),120,150	STD
MB841000	TC551001	128KX8	(80,100),120	STD
MB81C71A	TC5561/62	64KX1	25,30,(35)	HS
MB81C74	TC55416H	16KX4	(25),30,(35)	HS
MB81C75	TC55417H	16KX4 OE	(25),30,(35)	HS
MB81C78A	TC5588	8KX8	(35),45	HS
MB82B78	TC5588	8KX8	(15,20)	HS
MB81C79A	TC5589	8KX9	(35),45	HS
MB82B79	TC5589	8KX9	(15,20)	HS
MB81C84A	TC55464	64KX4	(25,35)	HS
MB82B84	TC55464	64KX4	15,(20)	HS
MB82B84	TC55B464	64KX4	(15),20	HS
MB82B85	TC55465	64KX4 OE	15,(20)	HS
MB82B85	TC55B465	64KX4 OE	(15),20	HS
MB8298	TC55328	32KX8	(25,35)	HS
MB82B88	TC55328	32KX8	15,(20)	HS
MB82B88	TC55B328	32KX8	(15),20	HS
MB8289	TC55329	32KX9	(25,35)	HS
MB82B89	TC55329	32KX9	15,(20)	HS
MB82B89	TC55B329	32KX9	(15),20	HS
MB82B008	TC55B8128	256KX4	25	HS

GOLDSTAR	TOSHIBA	DESCRIPTION	SPEED	CODE
GM76C88L	TC5565	8KX8	(150)	STD
GM76C256	TC55257	32KX8	(85,100),120	STD
GM76C8128	TC551001A	128KX8	(70,85,100)	STD

HS = High Speed STD = Standard Speed PS = Pseudo Static

HITACHI	TOSHIBA	DESCRIPTION	SPEED	CODE
HM6264A	TC5565	8KX8	(100,120,150)	STD
HM62256	TC55257	32KX8	(85,100),120,150	STD
HM628128	TC551001A	128KX8	(70,85,100),120	STD
HM6267	TC5561/62	64KX1	25,(35,45,55,70)	HS
HM6767	TC5561/62	64KX1	12,15,20,25,(35)	HS
HM6288	TC55416H	16KX4	(25,35)	HS
HM6788	TC55416H	16KX4	12,(15,20,25,35)	HS
HM6289	TC55417H	16KX4 OE	(25,35)	HS
HM6789	TC55417H	16KX4 OE	12,(15,20,25,35)	HS
HM6789	TC55B417	16KX4 OE	(12),15,20,25,35	HS
HM6208	TC55464	64KX4	(25,35),45	HS
HM6708	TC55464	64KX4	15,(20,25)	HS
HM6708	TC55B464	64KX4	(15),20,25	HS
HM6209	TC55465	64KX4 OE	(25,35),45	HS
HM6709	TC55465	64KX4 OE	15,(20,25)	HS
HM6709	TC55B465	64KX4 OE	(15),20,25	HS
HM62832	TC55328	32KX8	(25,35),45	HS
HM62A168	TC55188	4KX18X2	(25),35,45	HS
HM62A188	TC55188	4KX18X2	(25),35,45	HS
HM65256	TC51832	32KX8	(100,120),150,200	PS
HM658128	TC518129	128KX8	(100,120),150	PS

HYUNDAI	TOSHIBA	DESCRIPTION	SPEED	CODE
HY6264	TC5565	8KX8	70,85,(100,120,150)	STD
HY62C256	TC55257	32KX8	80,(100),120,150	STD
HY62256A	TC55257	32KX8	70,(100)	STD

IDT	TOSHIBA	DESCRIPTION	SPEED	CODE
IDT7187	TC5562	64KX1	15,20,25,(35)	HS
IDT7188	TC55416H	16KX4	(15,20,25,35)	HS
IDT71B88	TC55416H	16KX4	8,(10,12)	HS
IDT6198	TC55417H	16KX4 OE	(15,20,25,35)	HS
IDT61B98	TC55417H	16KX4 OE	8,(10,12)	HS
IDT7164	TC5588	8KX8	(15,20,25,35)	HS
IDT71B64	TC5588	8KX8	10,12,(15)	HS
IDT71B64	TC55B88	8KX8	(10,12),15	HS
IDT7169	TC5589	8KX9	(20,25,35)	HS
IDT71B69	TC5589	8KX9	12,(15,20)	HS
IDT71258	TC55464	64KX4	(20,25,35),45	HS
IDT71B258	TC55464	64KX4	12,15,(20)	HS
IDT71B258	TC55B464	64KX4	(12,15),20	HS
IDT61298	TC55465	64KX4 OE	(25,35),45	HS
IDT61B298	TC55465	64KX4 OE	12,15,(20)	HS
IDT61B298	TC55B465	64KX4 OE	(12,15),20	HS
IDT71256	TC55328	32KX8	(20,25,35),45	HS
IDT71B256	TC55328	32KX8	12,15,(20)	HS
IDT71B256	TC55B328	32KX8	(12,15),20	HS
IDT71259	TC55329	32KX9	(20,25,35)	HS

HS = High Speed STD = Standard Speed PS = Pseudo Static

INTEL	TOSHIBA	DESCRIPTION	SPEED	CODE
5164SL	TC5565	8KX8	(100,120)	STD
51256SL	TC55257	32KX8	70,(100)	STD
51018SL	TC551001	128KX8	(100,120)	STD
51C98	TC55416	16KX4	(25,35)	HS
5164	TC5588	8KX8	(20,25)	HS
51258	TC55464	64KX4	(25,35)	HS
51256	TC55328	32KX8	(25,35)	HS

LOGIC DEVICES	TOSHIBA	DESCRIPTION	SPEED	CODE
L7C187	TC5561/62	64KX1	20,25,(35,45)	HS
L7C164C	TC55416	16KX4	(20,25,35),45	HS
L7C166C	TC55417	16KX4 OE	(20,25,35),45	HS
L7C185C	TC5588	8KX8	(20,25,35),45	HS

MICRON TECH	TOSHIBA	DESCRIPTION	SPEED	CODE
MT5C6401	TC5561/62	64KX1	12,15,20,25,30,(35)	HS
MT5C6404	TC55416	16KX4	12,(15,20,25,30,35)	HS
MT5C6405	TC55417	16KX4 OE	12,(15,20,25,30,35)	HS
MT5C6405	TC55B417	16KX4 OE	(12),15,20,25,30,35	HS
MT5C6408	TC5588	8KX8	12,(15,20,25,30,35),45	HS
MT5C6408	TC55B88	8KX8	(12),15,20,25,30,35,45	HS
MT5C2564	TC55464	64KX4	15,(20,25,30,35),45	HS
MT5C2564	TC55B464	64KX4	(15),20,25,30,35,45	HS
MT5C2565	TC55465	64KX4 OE	15,(20,25,30,35),45	HS
MT5C2565	TC55B465	64KX4 OE	(15),20,25,30,35,45	HS
MT5C2568	TC55328	32KX8	15,(20,25,35),45	HS
MT5C2568	TC55B328	32KX8	(15),20,25,35,45	HS
MT56C0816	TC55187	4KX18X2	(20,25),35	HS

MITSUBISHI	TOSHIBA	DESCRIPTION	SPEED	CODE
M5M5165	TC5565	8KX8	70,(100,120,150)	STD
M5M5255	TC55257	32KX8	(70,85,100),120,150	STD
M5M5256	TC55257	32KX8	(70,85,100),120,150	STD
M5M51008	TC551001A	128KX8	(70,85,100),120	STD
M5M5187	TC5561/62	64KX1	15,20,25,35,(45,55)	HS
M5M5188	TC55416	16KX4	(15,20,25,35),45,55	HS
M5M5189	TC55417	16KX4 OE	(15,20,25,35),45,55	HS
M5M5178	TC5588	8KX8	(35),45,55	HS
M5M5179	TC5589	8KX9	(35),45,55	HS
M5M5258	TC55464	64KX4	15,(20,25,30,35),45	HS
M5M5258	TC55B464	64KX4	(15),20,25,30,35,45	HS

MOSEL	TOSHIBA	DESCRIPTION	SPEED	CODE
MS6264	TC5565	8KX8	70,(100)	STD
MS6264C	TC5565	8KX8	80,(100),150	STD
MS62256	TC55257	32KX8	70,(85,100)	STD
MS62256B	TC55257	32KX8	70,(100),120,150	STD
MS631000	TC551001	128KX8	80,(100),120	STD
MS6264A	TC5588	8KX8	45,55	HS
MS62256A	TC55328	32KX8	(25,35),45,55	HS

HS = High Speed STD = Standard Speed PS = Pseudo Static

MOTOROLA	TOSHIBA	DESCRIPTION	SPEED	CODE
MCM60256A	TC55257	32KX8	(85,100),120	STD
MCM60L256A	TC55257	32KX8	70,(85,100),120	STD
MCM6287	TC5561/62	64KX1	12,15,20,25,(35)	HS
MCM6288	TC55416H	16KX4	12,(15,20,25,35)	HS
MCM6290	TC55417H	16KX4 OE	12,(15,20,25,35)	HS
MCM6264	TC5588	8KX8	(15,20,25,35),45	HS
MCM6265	TC5589	8KX9	(15,20,25)	HS
MCM6208	TC55464	64KX4	15,(20,25,35)	HS
MCM6208	TC55B464	64KX4	(15),20,25,35	HS
MCM6708	TC55B464	64KX4	(10,12,15)	HS
MCM6209	TC55465	64KX4 OE	15,(20,25,35)	HS
MCM6209	TC55B465	64KX4 OE	(15),20,25,35	HS
MCM6709	TC55B465	64KX4 OE	(10,12,15)	HS
MCM6206	TC55328	32KX8	(17,20,25,35),45	HS
MCM6706	TC55B328	32KX8	(10,12,15)	HS
MCM6205	TC55329	32KX9	(17,20,25,35),45	HS
MCM51L8128	TC518128	128KX8	80,(100)	PS
MCM51LV8128	TC518128LV	128KX8LV	80,(100)	PS
MCM51L8129	TC518129	128KX8	80,(100)	PS
MCM51LV8129	TC518129LV	128KX8LV	80,(100)	PS

NEC	TOSHIBA	DESCRIPTION	SPEED	CODE
uPD4364	TC5565	8KX8		STD
uPD43256A	TC55257	32KX8	(85,100,120),150	STD
uPD43256B	TC55257	32KX8	55,70,(85)	STD
uPD431000	TC551001A	128KX8	(85,100),120	STD
uPD431000A	TC551001A	128KX8	(70,85)	STD
uPD4361	TC5561	64KX1	40,45,(55,70)	HS
uPD4361	TC5561/62	64KX1	(40,45),55,70	HS
uPD4362	TC55416H	16KX4	12,(15,20,25,35)	HS
uPD4363	TC55417H	16KX4 OE	12,(15,20,25,35)	HS
uPD4363	TC55B417	16KX4 OE	(12,)15,20,25,35	HS
uPD4368	TC5588	8KX8	(15,20,25,35)	HS
uPD4369	TC5589	8KX9	(15,20,25,35)	HS
uPD43254	TC55464	64KX4	15,(20,25,35),45	HS
uPD43254	TC55B464	64KX4	(15),20,25,35,45	HS
uPD43253	TC55465	64KX4 OE	15,(20,25,35),45	HS
uPD43253	TC55B465	64KX4 OE	(15),20,25,35,45	HS
uPD43258	TC55328	32KX8	(20,25,35),45	HS
uPD43259	TC55329	32KX9	(20,25,35),45	HS

OKI	TOSHIBA	DESCRIPTION	SPEED	CODE
MSM5165	TC5565	8KX8	(100,120,150)	STD
MSM51257	TC55257	32KX8	(85,100,120)	STD
MSM5188	TC55416	16KX4	45,55,70	HS

HS = High Speed STD = Standard Speed PS = Pseudo Static

PARADIGM	TOSHIBA	DESCRIPTION	SPEED	CODE
PDM41258	TC55464	64KX4	10,12,15,(20,25)	HS
PDM41258	TC55B464	64KX4	(10,12,15),20,25	HS
PDM41298	TC55465	64KX4 OE	10,12,15,(20,25)	HS
PDM41298	TC55B465	64KX4 OE	(10,12,15),20,25	HS
PDM41256	TC55328	32KX8	10,12,15,(20,25)	HS
PDM41256	TC55B328	32KX8	(10,12,15),20,25	HS
PDM41259	TC55329	32KX9	10,12,15,(20,25)	HS
PDM41259	TC55B329	32KX9	(10,12,15),20,25	

PERFORMANCE	TOSHIBA	DESCRIPTION	SPEED	CODE
P4C187	TC5562	64KX1	10,12,15,20,25,(35)	HS
P4C188	TC55416H	16KX4	12,(15,20,25,35)	HS
P4C198	TC55417H	16KX4 OE	12,(15,20,25,35)	HS
P4C198	TC55B417	16KX4 OE	(12),15,20,25,35	HS
P4C164	TC5588	8KX8	(15,20,25),30,(35)	HS
P4C163	TC5589	8KX9	(20,25,35)	HS
P4C1258	TC55464	64KX4	(20,25,35)	HS
P4C1298	TC55465	64KX4 OE	(20,25,35)	HS
P4C1256	TC55328	32KX8	(20,25,35)	HS

SAMSUNG	TOSHIBA	DESCRIPTION	SPEED	CODE
KM6264	TC5565	8KX8	70,(100,120)	STD
KM62256	TC55257	32KX8	80,(100),120	STD
KM681000	TC551001	128KX8	(70,85,100),120	STD
KM6165A	TC5561/62	64KX1	25,(35,45)	HS
KM6465A	TC55416H	16KX4	(25,35),45	HS
KM64B65	TC55416H	16KX4	(15,20)	HS
KM6466A	TC55417H	16KX4 OE	(25,35),45	HS
KM6865A	TC5588	8KX8	(15,20,25)	HS
KM64257A	TC55464	64KX4	(25,35),45	HS
KM68257A	TC55328	32KX8	15,(20,25,35)	HS
KM68257A	TC55B328	32KX8	(15),20,25,35	HS
KM641001	TC55B4256	256KX4	(20),25,35	HS
KM658128	TC518128	128KX8	(80,100,120)	PS

SHARP	TOSHIBA	DESCRIPTION	SPEED	CODE
LH5160	TC5565	8KX8	(100)	STD
LH52256	TC55257	32KX8	70,(90),120	STD
LH511000	TC551001	128KX8	(100),120	STD
LH5261	TC5562	64KX1	25,(35)	HS
LH5267A	TC55417H	16KX4 OE	(20,25)	HS
LH52252A	TC55464	64KX4	(25,35),45	HS
LH52252B	TC55464	64KX4	15,(20)	HS
LH52252B	TC55B464	64KX4	(15),20	HS
LH52253	TC55465	64KX4 OE	15,(20)	HS
LH52253	TC55B465	64KX4 OE	(15),20	HS
LH52258	TC55328	32KX8	(35),45	HS
LH52258A	TC55328	32KX8	15,(20,25)	HS
LH52258A	TC55B328	32KX8	(15),20,25	HS

HS = High Speed STD = Standard Speed PS = Pseudo Static

S-MOS	TOSHIBA	DESCRIPTION	SPEED	CODE
SRM2264	TC5565	8KX8	(100,120)	STD
SRM20256	TC55257	32KX8	(85,100),120	STD
SRM201000	TC551001	128KX8	(85,100)	STD
SRM21256	TC55464	64KX4	45,55	HS
SRM22256	TC55328	32KX8	55,70	HS

SONY	TOSHIBA	DESCRIPTION	SPEED	CODE
CXK5864	TC5565	8KX8	70,(100,120)	STD
CXK58257	TC55257	32KX8	70,(85,100),120	STD
CXK581001	TC551001A	128KX8	(70,85)	STD
CXK581000	TC551001A	128KX8	(100),120,150	STD
CXK5164	TC5562	64KX1	25,30,(35)	HS
CXK5464	TC55416	16KX4	(25),30,(35)	HS
CXK5465	TC55417	16KX4 OE	(25),30,(35)	HS
CXK5863	TC5588	8KX8	(20,25),30,(35)	HS
CXK5866	TC55B88	8KX8	(12),15,20	HS
CXK5866	TC5588	8KX8	12,(15,20)	HS
CXK5971	TC5589	8KX9	(25),30,(35)	HS
CXK5972	TC5589	8KX9	12,(15,20)	HS
CXK54256	TC55464	64KX4	(35),45,55	HS
CXK58258	TC55328	32KX8	(35),45,55	HS
CXK58258A	TC55328	32KX8	15,(20,25)	HS
CXK58258A	TC55B328	32KX8	(15),20,25	HS
CXK59288	TC55329	32KX9	15,(20,25)	HS
CXK59288	TC55B329	32KX9	(15),20,25	HS
CXK7701	TC55187	4KX18X2	(30),35,45,55	HS
CXK7701A	TC55187	4KX18X2	(25),35,45	HS

UMC	TOSHIBA	DESCRIPTION	SPEED	CODE
UM6264	TC5565	8KX8	70,(100,120)	STD
UM62256	TC55257	32KX8	(100),120,150	STD
UM621024	TC551001A	128KX8	55,(70)	STD
UM6164	TC5588	8KX8	(20,25),30	HS
UM61168	TC55187	4KX18X2	(25),35,45	HS

VITELLIC	TOSHIBA	DESCRIPTION	SPEED	CODE
V63C64	TC5588	8KX8	(25),30,(35),45,55	HS
V63C71	TC55464	64KX4	15,(20,25,35)	HS
V63C71	TC55B464	64KX4	(15),20,25,35	HS
V63C70	TC55465	64KX4 OE	(15,20,25,35)	HS
V63C70	TC55B465	64KX4 OE	(15),20,25,35	HS
V6C330	TC55187	4KX18X2	(25,30),35,45	HS
V6C328	TC55188	4KX18X2	(30),40,45	HS

HS = High Speed STD = Standard Speed PS = Pseudo Static

CMOS Pseudo Static RAM

32,768 WORD x 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51832 Family is a 256K bit high-speed CMOS Pseudo-Static RAM organized as 32,768 words by 8 bits. The TC51832 Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{OE}/RFSH$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC51832 Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC51832 Family is pin-compatable with the 256K bit static RAM. The TC51832P is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC51832F is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

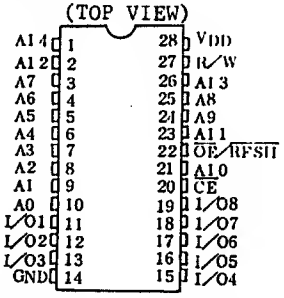
FEATURES

- Organization: 256K bit(32,768 word × 8 bit)
- Fast Access Time and Low Power Dissipation

	TC51832P Family		
	-85	-10	-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns
P_D -Operating- Max.	303mW	248mW	220mW
Self Refresh Current	1mA/100μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs: TTL compatible
- 256 refresh cycle/4ms
- Pin Compatible: 256K SRAM TC55257
- Logic Compatible: SRAM R/W Pin
- 28 pin Standard Plastic PKG
  P/PL : 600 mil DIP
  SP/SPL: 300 mil DIP
  F/FL : 450 mil SOP

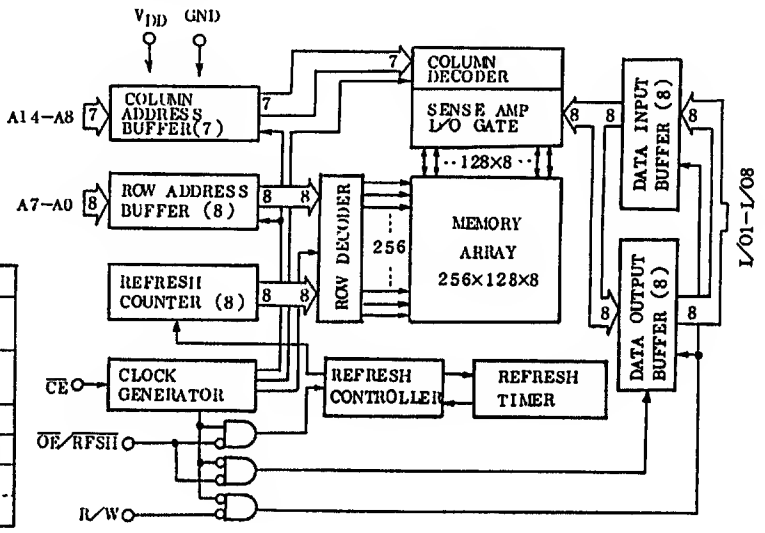
PIN CONNECTION



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable/ Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	-1.0∿7.0	V	1
V_{OUT}	Output Voltage	-1.0∿7.0	V	1
V_{DD}	Power Supply Voltage	-1.0∿7.0	V	1
T_{OPR}	Operating Temperature	0∿70	°C	1
T_{STG}	Storage Temperature	-55∿150	°C	1
T_{SOLDER}	Soldering Temperature·Time	260・10	°C·sec	1
P_D	Power Dissipation	600	mW	1
I_{OUT}	Short Circuit Output Current	50	mA	1

DC RECOMMENDED OPERATING CONDITIONS (Ta=0∿70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0∿70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address Cycling: t_{RC}=t_{RC} MIN.	135ns	-	55	mA	3,4
		160ns	-	45		
		190ns	-	40		
I_{DDS1}	Standby Current 1 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH}	TC51832P/SP/F	-	2	mA	
		TC51832PL/SPL/FL	-	1		
I_{DDS2}	Standby Current 2 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{DD}-0.2V	TC51832P/SP/F	-	1	mA	
		TC51832PL/SPL/FL	-	100	μA	
I_{DDF}	Self Refresh Current $\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V	TC51832P/SP/F	-	1	mA	
		TC51832PL/SPL/FL	-	100	μA	
$I_{I(L)}$	Input Leakage Current 0V≦V_{IN}≦V_{DD}, All other inputs not under test=0V		-10	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, 0V≦V_{OUT}≦V_{DD}		-10	10	μA	
V_{OH}	Output High Level I_{OUT}=-5mA		2.4	-	V	
V_{OL}	Output Low Level I_{OUT}=4.2mA		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0~70°C) (NOTES:5,6,7,8,9)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write Enable	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ to $\overline{CE}$ Active Delay Time	160	-	190	-	225	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8000	-	8000	-	8000	-	ns	13
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	13

(Continued)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V, f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A0 ∿ A14)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	-	7	pF
C_{IO}	Input/Output Capacitance (I/O1 ∿ I/O8)	-	7	pF

NOTE) This parameter is periodically sampled and is not 100% tested.

NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) IDDO depends on cycle rate.

4) IDDO depends on output loading. Specified values are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RFSH}$ are required after power-up, before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input ($\overline{OE}$) and refresh control input ($\overline{RFSH}$) under the condition of that $\overline{CE}$=V_{IL} and $\overline{CE}$=V_{IH}, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).

12) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all the address inputs must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are defined by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}$=V_{IH}.

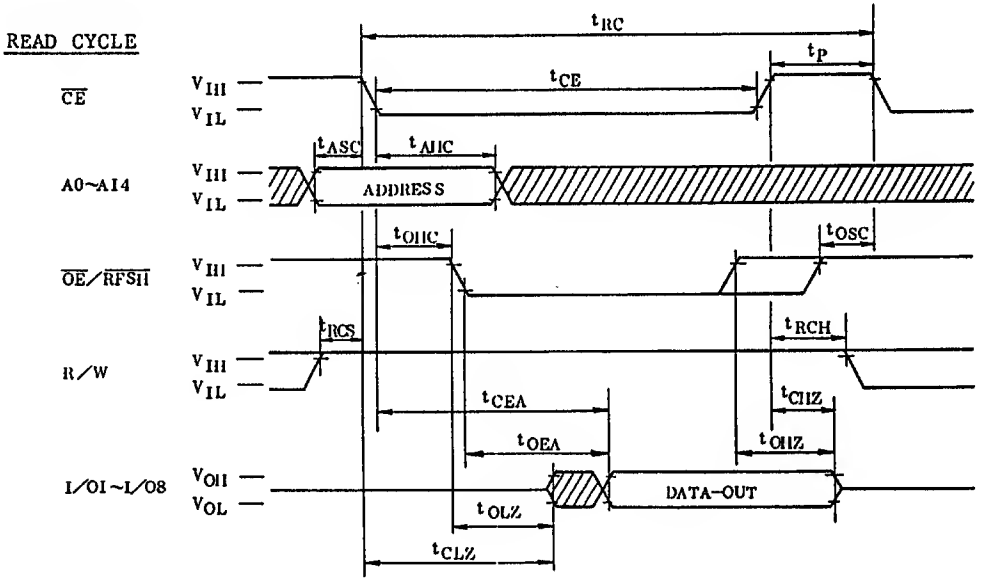
    Auto refresh: $\overline{OE}/\overline{RFSH}$ pulse width$\leqq$tFAP (max.)
    Self refresh: $\overline{OE}/\overline{RFSH}$ pulse width$\geqq$tFAS (min.)

The following timing parameter must be kept for proper device operation after refresh

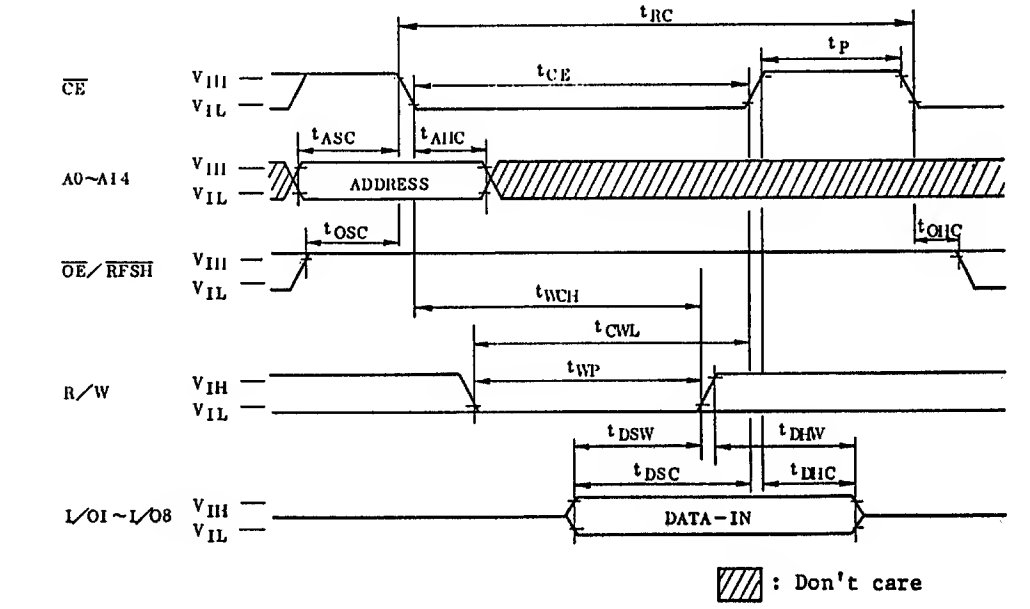
    Auto refresh: tFCE
    Self refresh: tFRS

TIMING CHART

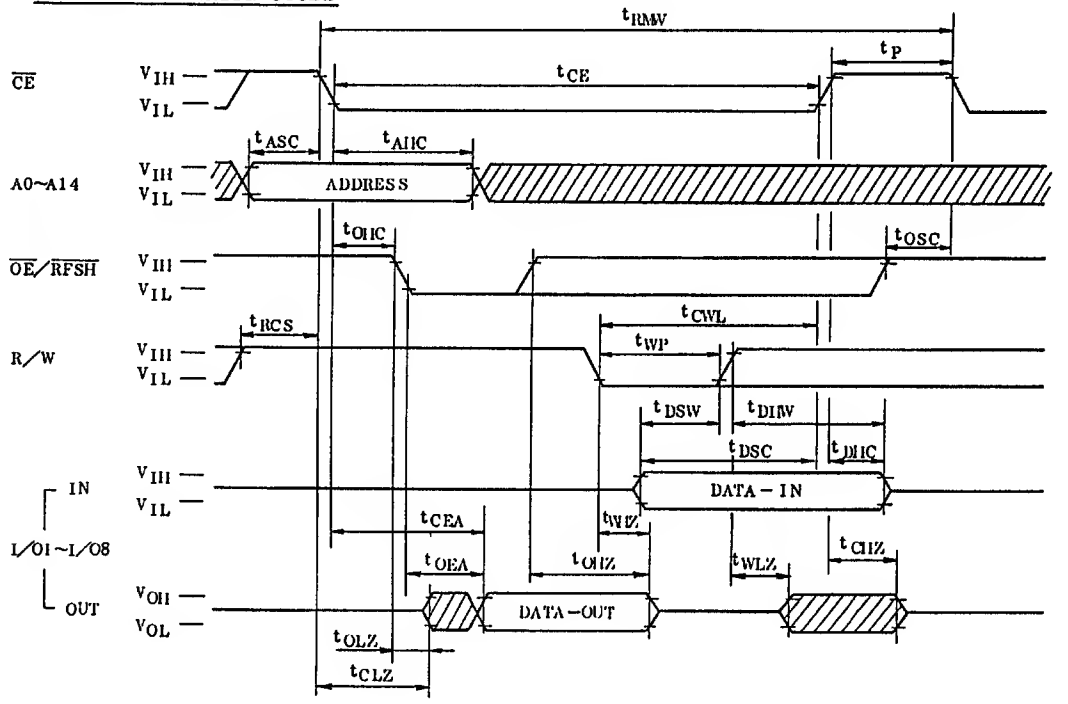
READ CYCLE



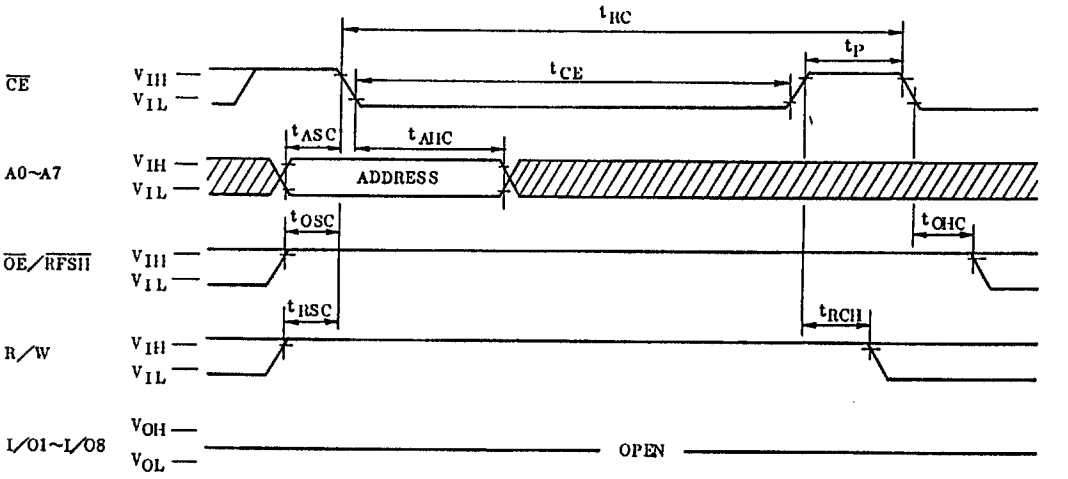
WRITE CYCLE



READ MODIFY WRITE CYCLE

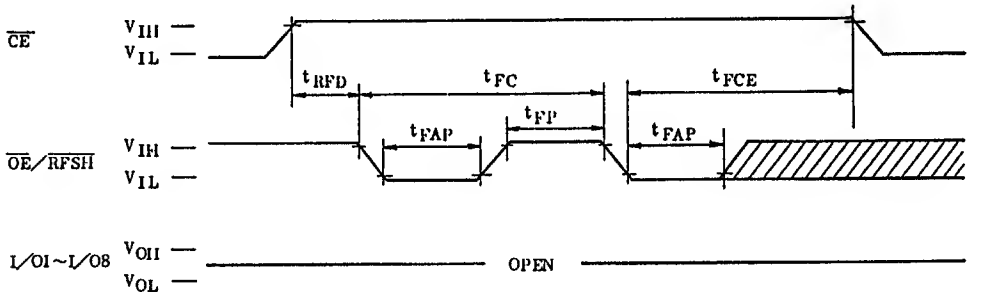


CE ONLY REFRESH CYCLE



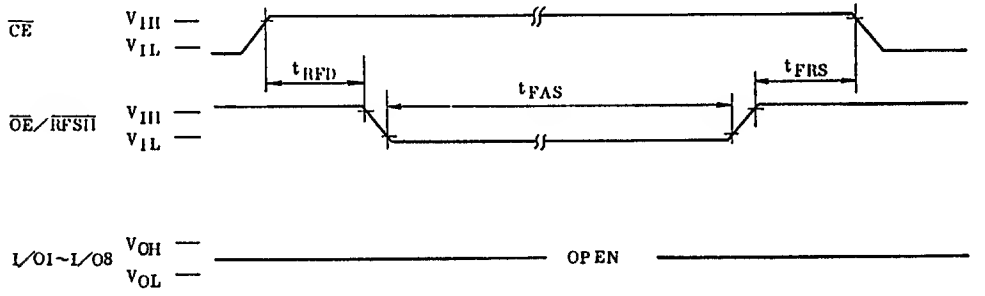
▨ : Don't care

AUTO REFRESH CYCLE



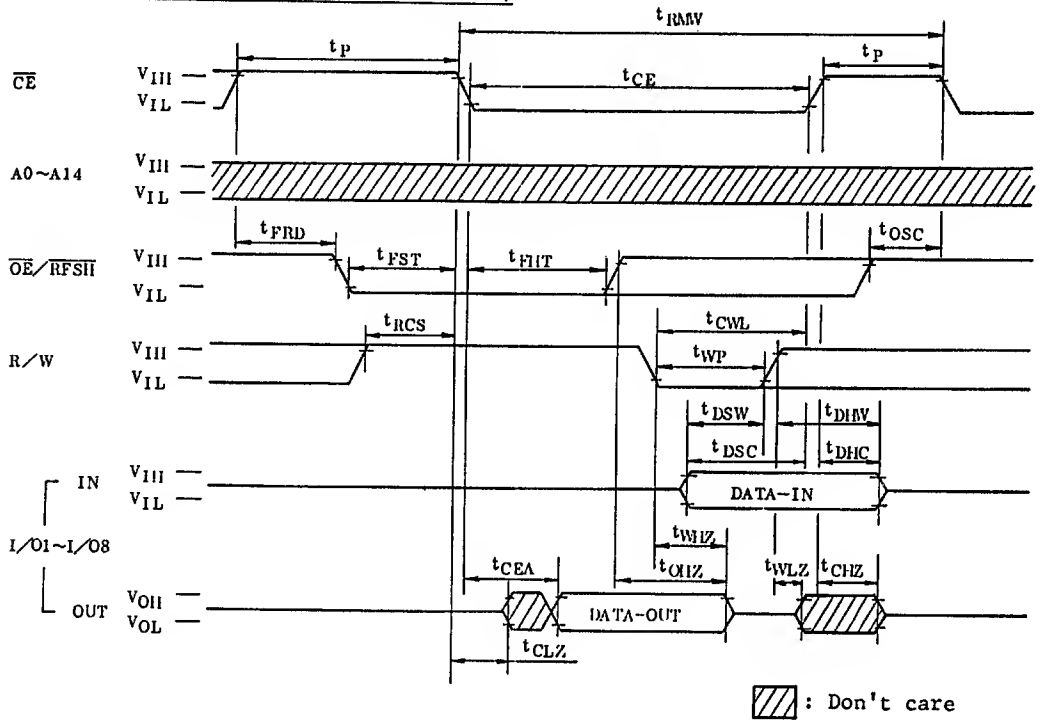
Note) A0 ∿ A14, R/W=Don't care ▨: Don't care

SELF REFRESH CYCLE



Note) A0 ∿ A14, R/W=Don't care

REFRESH COUNTER TEST CYCLE (READ WRITE)



REFRESH COUNTER TEST

The internal refresh operation of TC51832P family can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.

The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

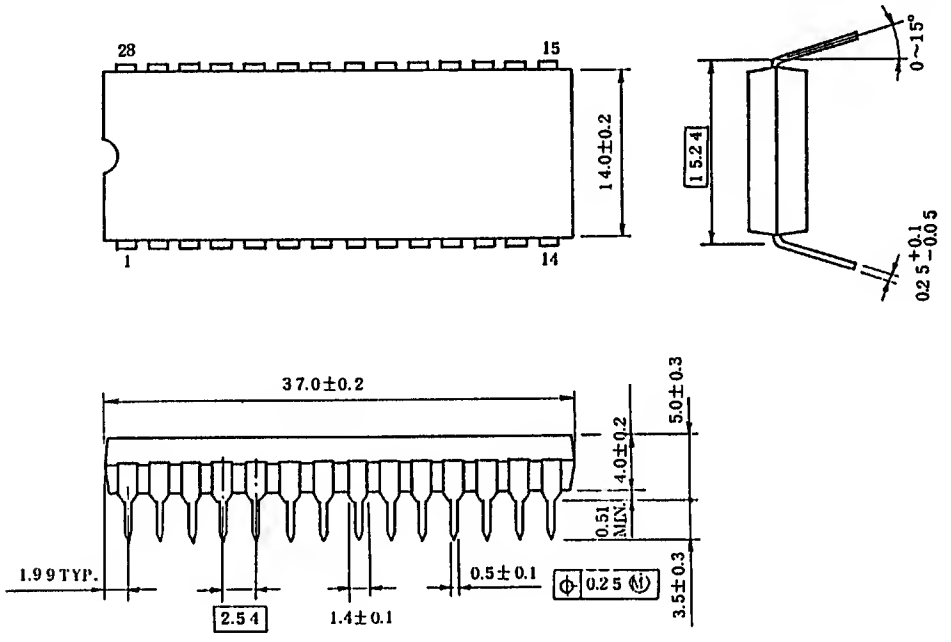
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (DIP28-P-600)

Unit in mm



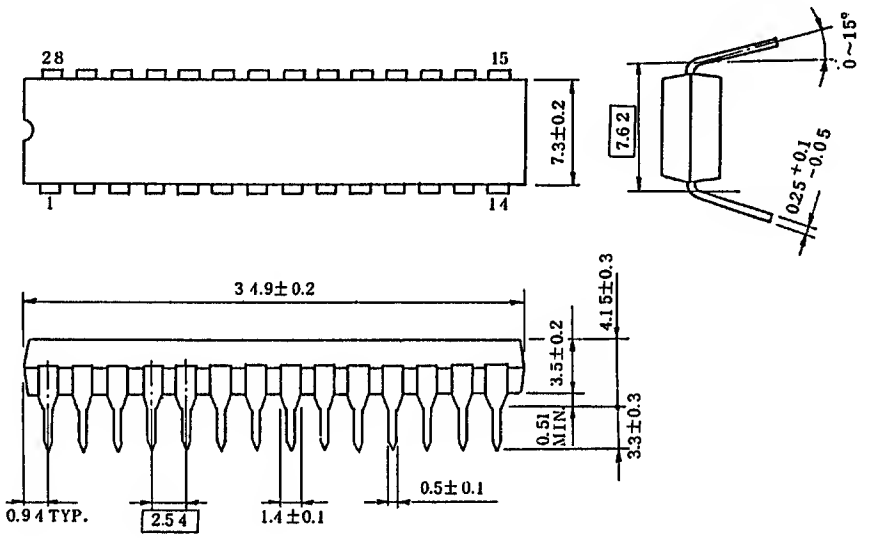
NOTES: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832P-85, TC51832PL-85
TC51832P-10, TC51832PL-10
TC51832P-12, TC51832PL-12

OUTLINE DRAWINGS (DIP28-P-300)

Unit in mm



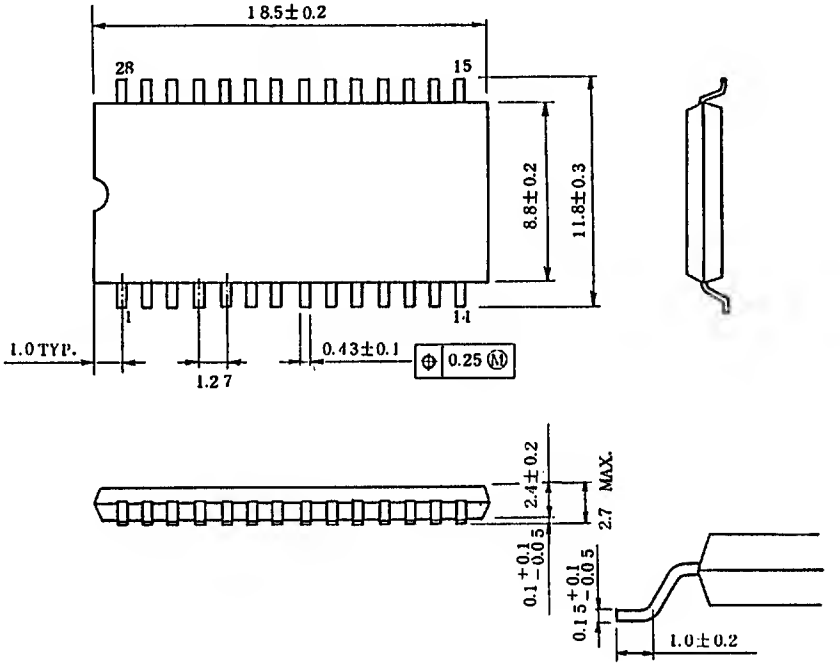
Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832SP-85, TC51832SPL-85
TC51832SP-10, TC51832SPL-10
TC51832SP-12, TC51832SPL-12

OUTLINE DRAWINGS (SOP28-P-450)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832F-85, TC51832FL-85
TC51832F-10, TC51832FL-10
TC51832F-12, TC51832FL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518128A Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518128A Family has a static RAM-like write functionality where input data is written into the memory cell at the rising edge of R/W, which allows easy interfacing with microprocessor.

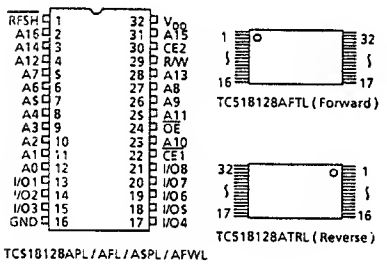
The TC518128A Family is a pin-compatible with 1M bit CMOS Static RAM - JEDEC standard and is packaged in a 32 pin standard 0.6 inch and 0.3 inch width plastic DIP and small-out line plastic flat package and a 32 pin plastic thin small-cut-line package (forward, reverse type).

FEATURES

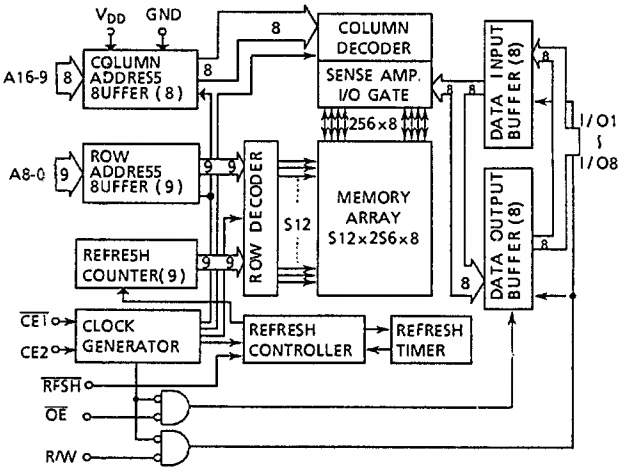
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Single Power Supply : 5V±10%
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle/8ms
- Auto refresh power down function
- Pin Compatible : 1M SRAM (JEDEC)
- Logic Compatible : SRAM R/W Pin
- Logic Compatible : SRAM R/W Pin
- Package: TC518128AP/APL : DIP32-P-600
  TC518128AF/AFL : SOP32-P-450
  TC518128ASP/ASPL : DIP32-P-300B
  TC518128AFW/AFWL : SOP32-P-525
  TC518128AFTL : TSOP32-P-0820
  TC518128ATRL : TSOP32-P-0820A

	TC518128A Family		
	-80	-10	-12
t_{CEA} CE Access Time	80ns	100ns	120ns
t_{OEA} OE Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (L version)		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ -1.0V)
* ··· Don't care (6.5V ~ -1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	-1.0~7.0	V	1
V_{OUT}	Output Voltage	-1.0~7.0	V	
V_{DD}	Power Supply Voltage	-1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	-55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3, 4
		100ns version	–	40	60		
		120ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IH}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDS2}	Standby Current $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = V_{DD} – 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IL}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE1}$, CE2, Address cycling : tRC = tRC min)	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}		– 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = – 5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

Note) In I_{DDS1} and I_{DDF1} with $\overline{CE1}$=V_{IH}(CE2=V_{IL}), these specification limits are guaranteed under the condition of CE2=V_{IH} or CE2=V_{IL}($\overline{CE1}$=V_{IH} or $\overline{CE1}$=V_{IL}). In I_{DDS2} and I_{DDF2} with $\overline{CE1}$≧V_{DD}–0.2V(CE2≦0.2V), theses specification are guaranteed under the condition of CE2≧V_{DD}–0.2V or CE2≦0.2V($\overline{CE1}$≧V_{DD}–0.2V or $\overline{CE1}$≦0.2V).

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input / Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

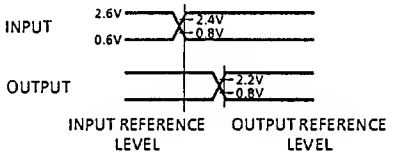
(V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C) (NOTES : 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	CE Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-2	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-2	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-2	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from CE	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time form $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t_{CES}	CE2 Low Set-Up Time	5	–	5	–	5	–	ns	14
t_{CEH}	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

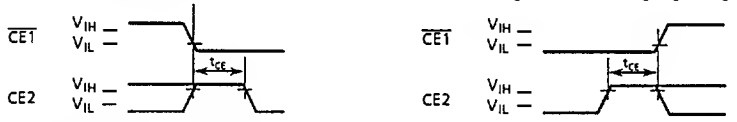
NOTES:

1) Stress greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

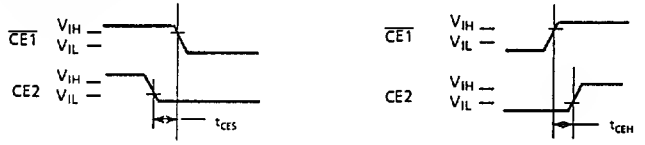
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.
    Auto refresh : $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{RFSH}$ = "L" after power-up
13) The timings, t_{CE} (min.) and t_{CE} (max.), must be kept for device proper operation as follows.

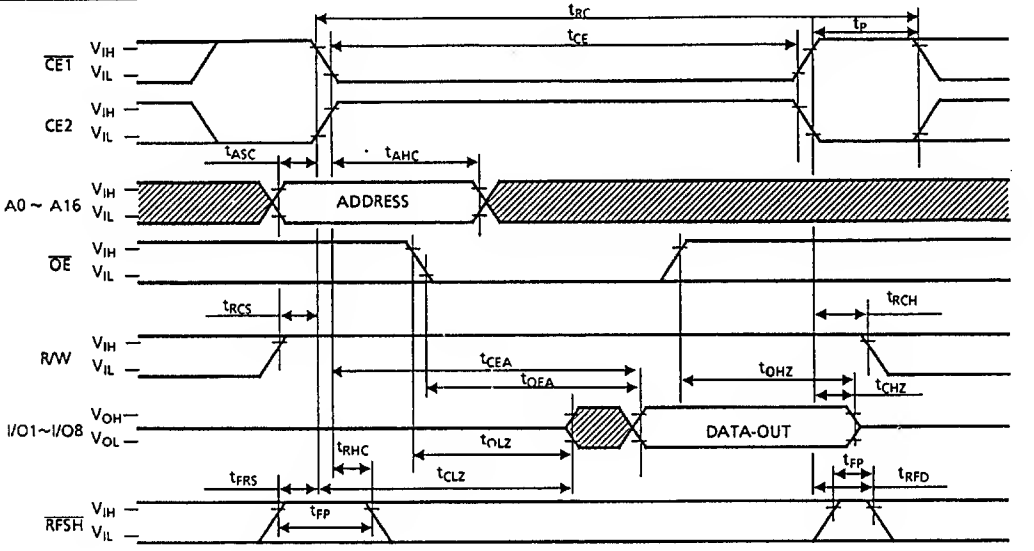


14) The timings, t_{CES} (min.) and t_{CEH} (min.), must be kept for using $\overline{CE1}$ and CE2 at the same clock as follow.

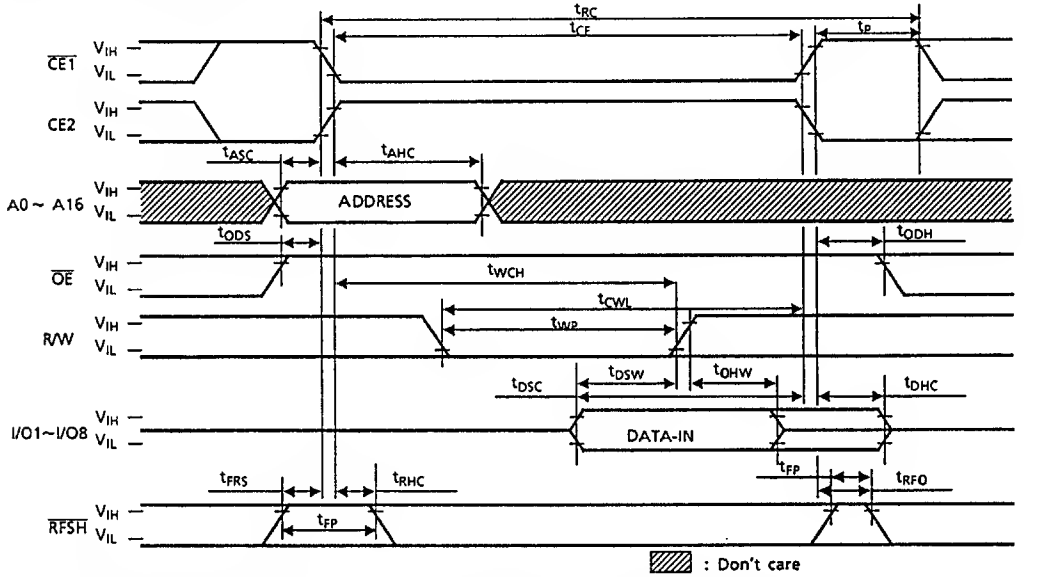


TIMING WAVEFORMS

READ CYCLE

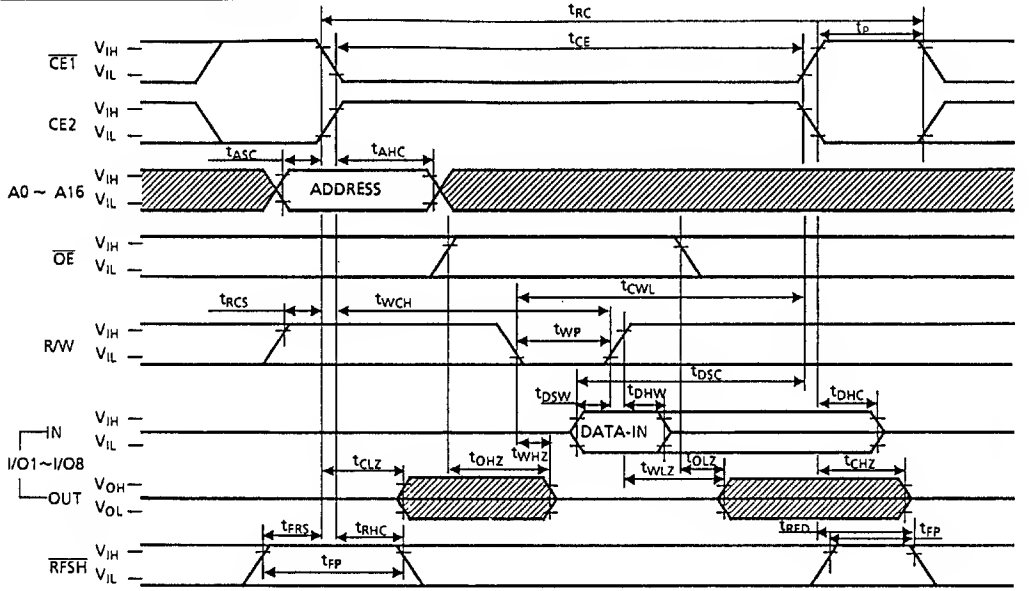


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

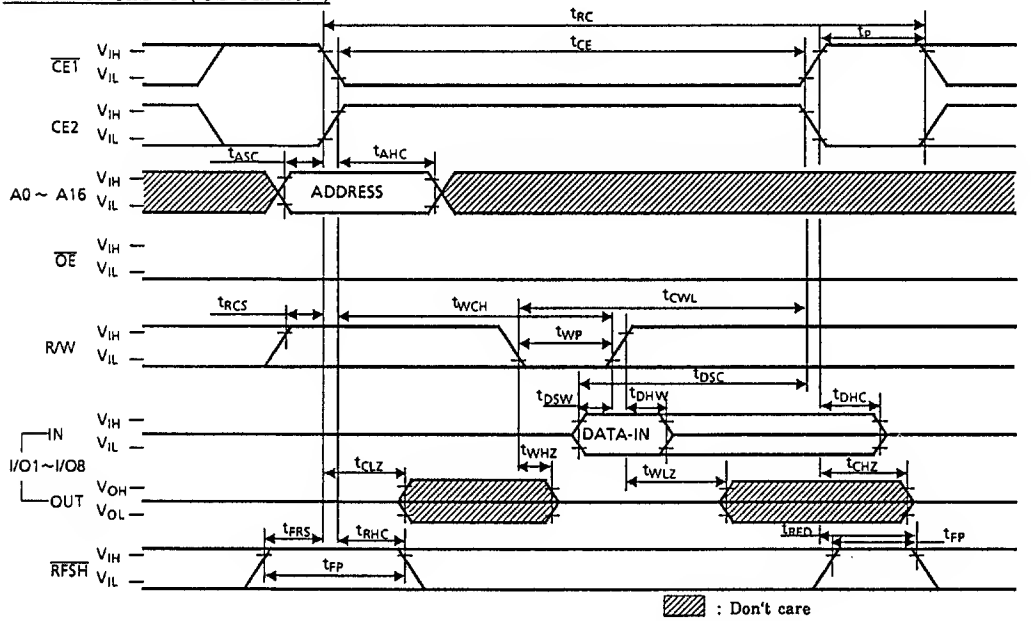


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

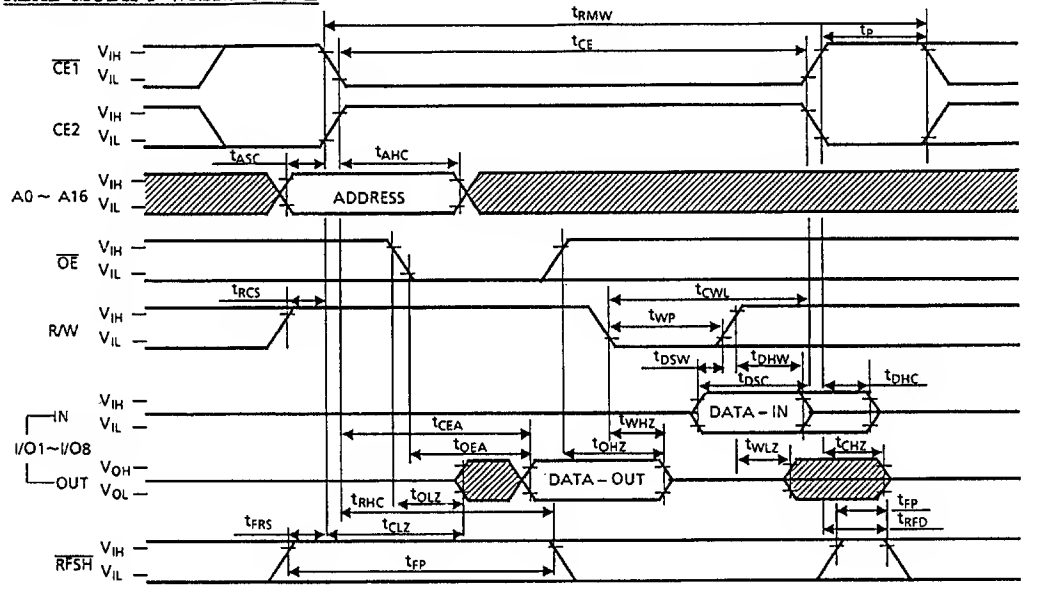


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

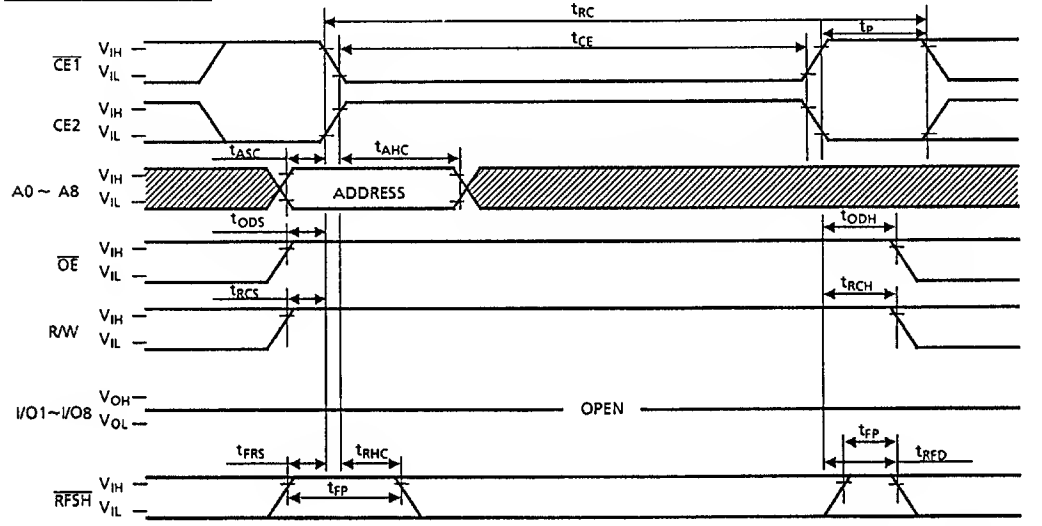


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

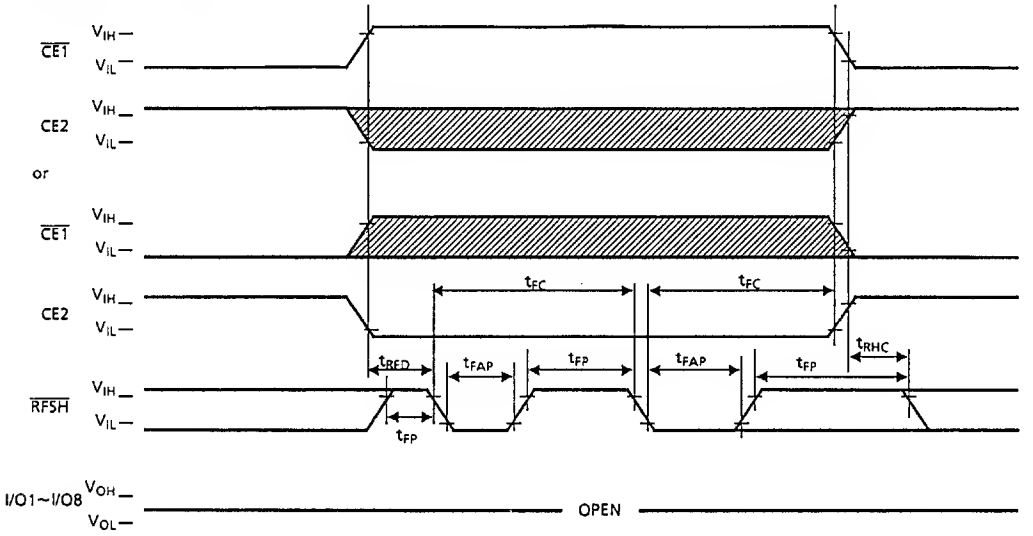


Note : A9 ~ A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

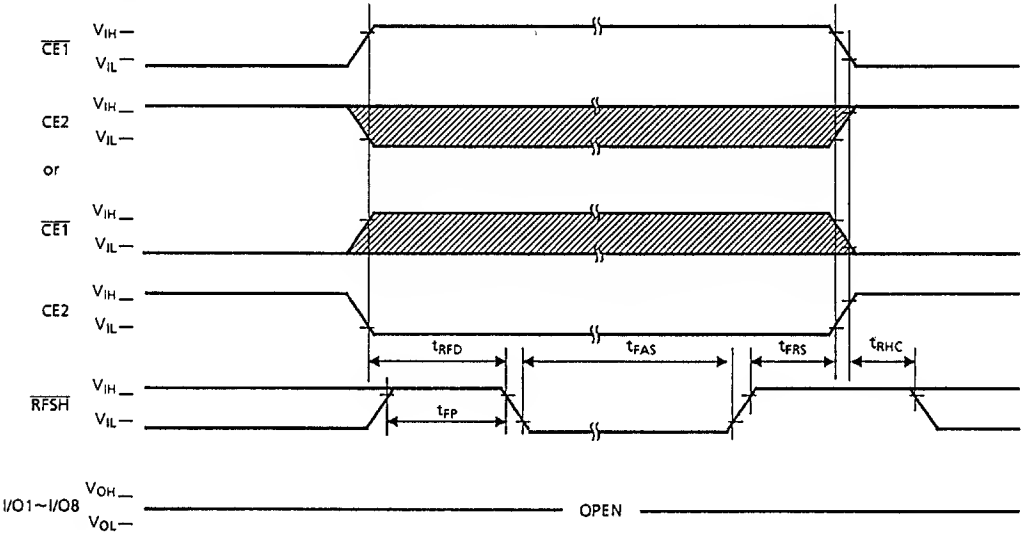
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

SELF REFRESH

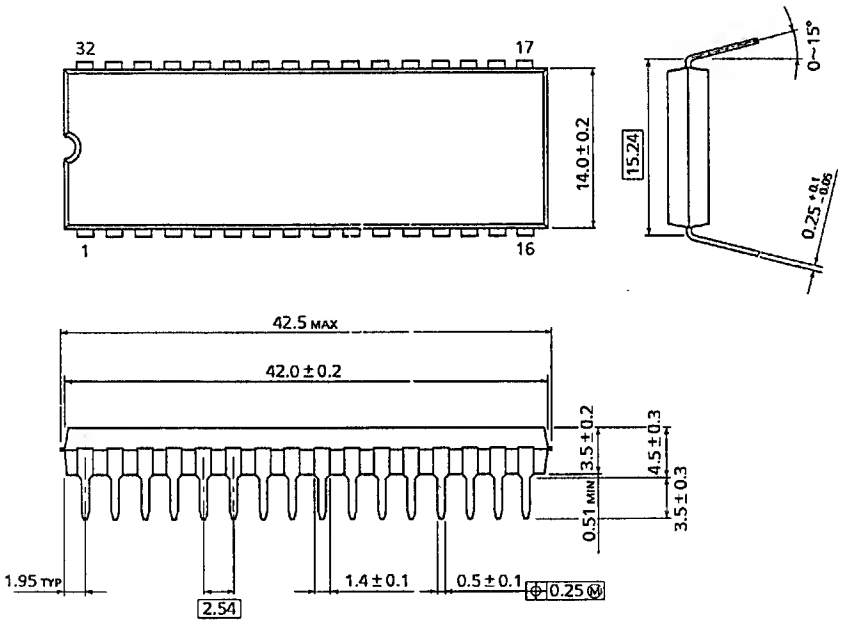


NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

OUTLINE DRAWING (DIP32 - P - 600)

Unit in mm

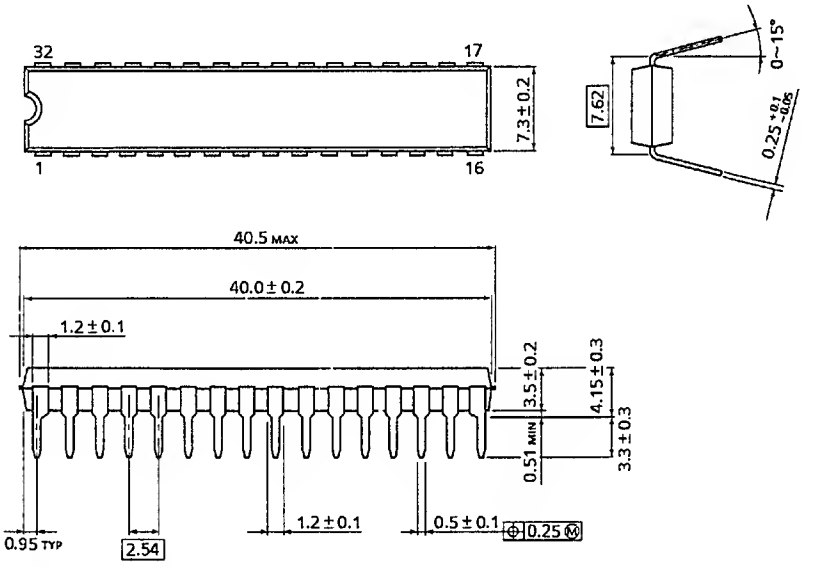


Weight : 4.53 g (Typ.)

TC518128AP-80, TC518128APL-80
TC518128AP-10, TC518128APL-10
TC518128AP-12, TC518128APL-12

OUTLINE DRAWING (DIP32 − P − 300)

Unit in mm

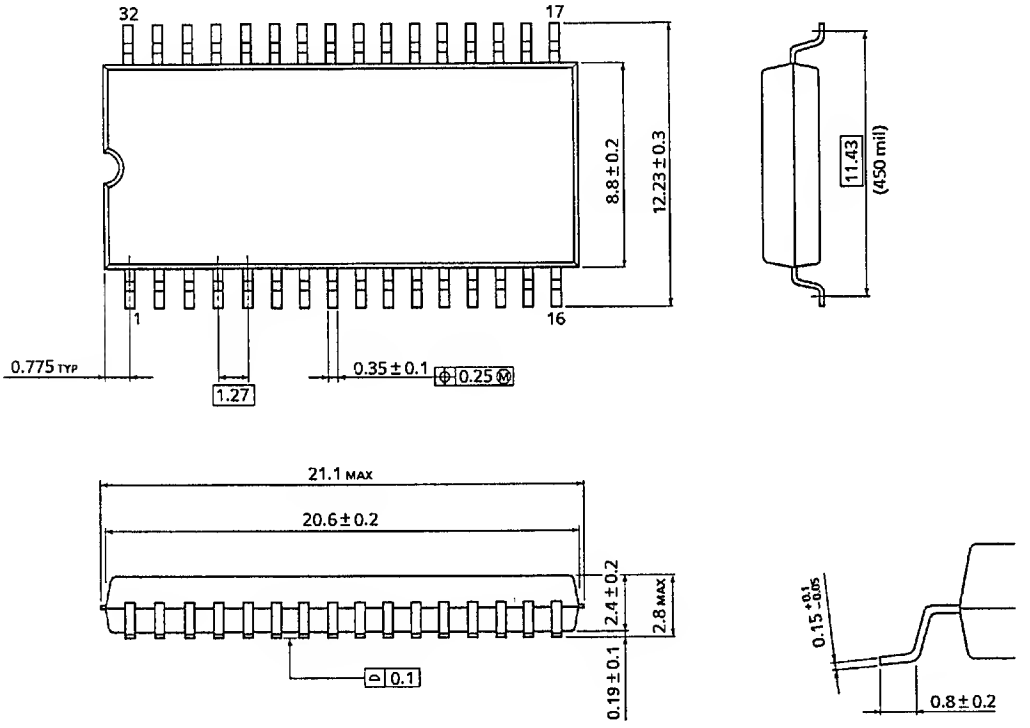


Weight : 2.36 g (Typ.)

TC518128ASP-80, TC518128ASPL-80
TC518128ASP-10, TC518128ASPL-10
TC518128ASP-12, TC518128ASPL-12

OUTLINE DRAWING (SOP32 – P – 450)

Unit in mm

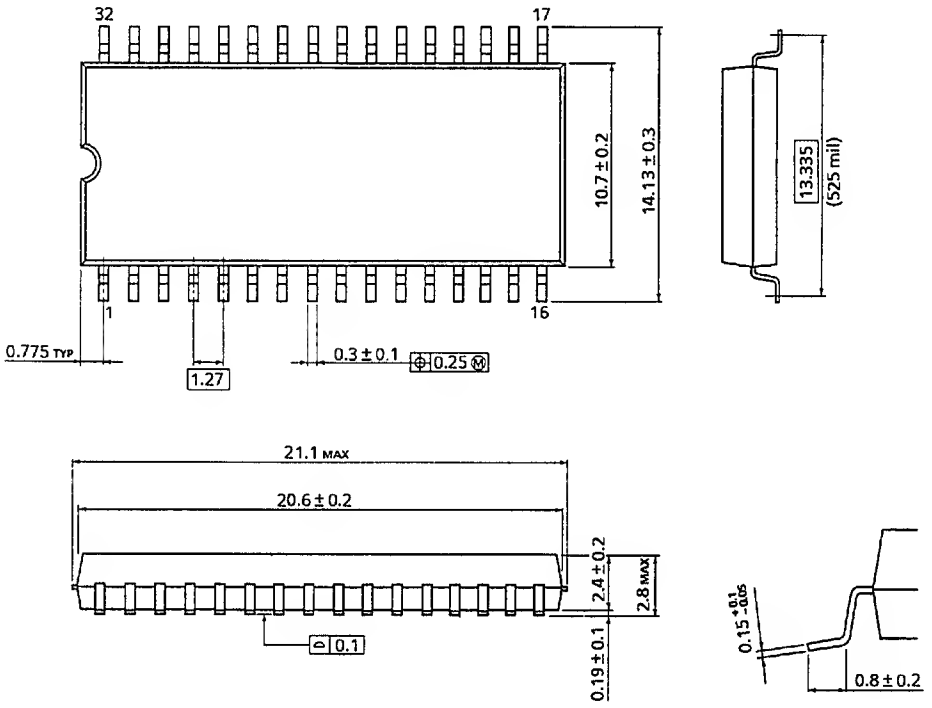


Weight : 0.87 g (Typ.)

TC518128AF-80, TC518128AFL-80
TC518128AF-10, TC518128AFL-10
TC518128AF-12, TC518128AFL-12

OUTLINE DRAWING (SOP32 − P − 525)

Unit in mm



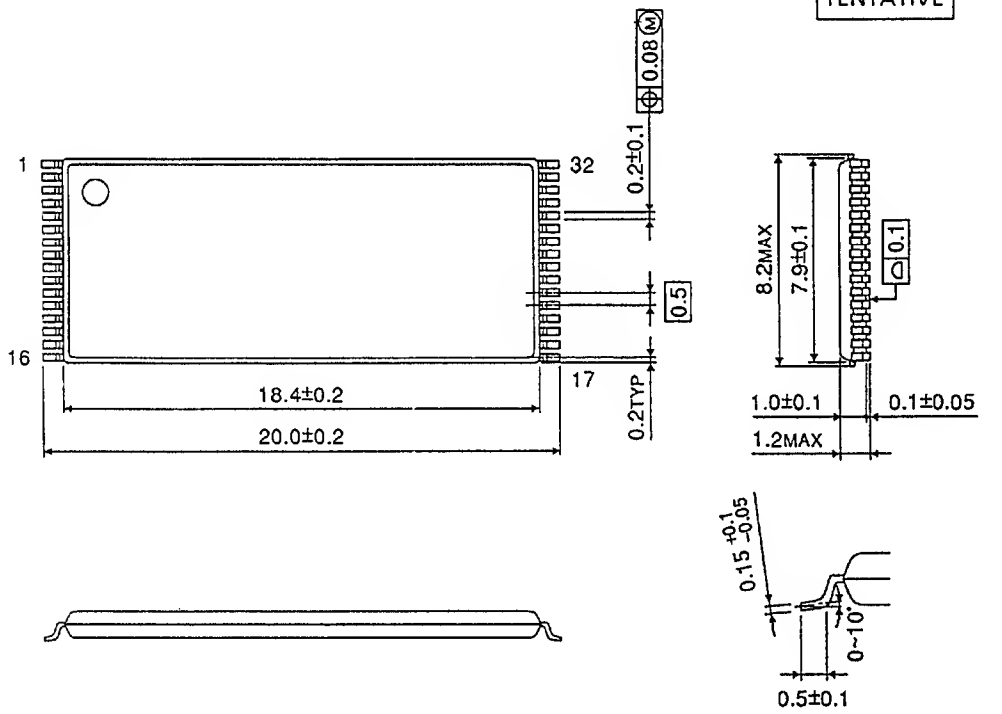
Weight : 1.10 g (Typ.)

TC518129AFW-80, TC518129AFWL-80
TC518129AFW-10, TC518129AFWL-10
TC518129AFW-12, TC518129AFWL-12

OUTLINE DRAWING (TSOP32 - P - 0820)

Unit in mm

TENTATIVE



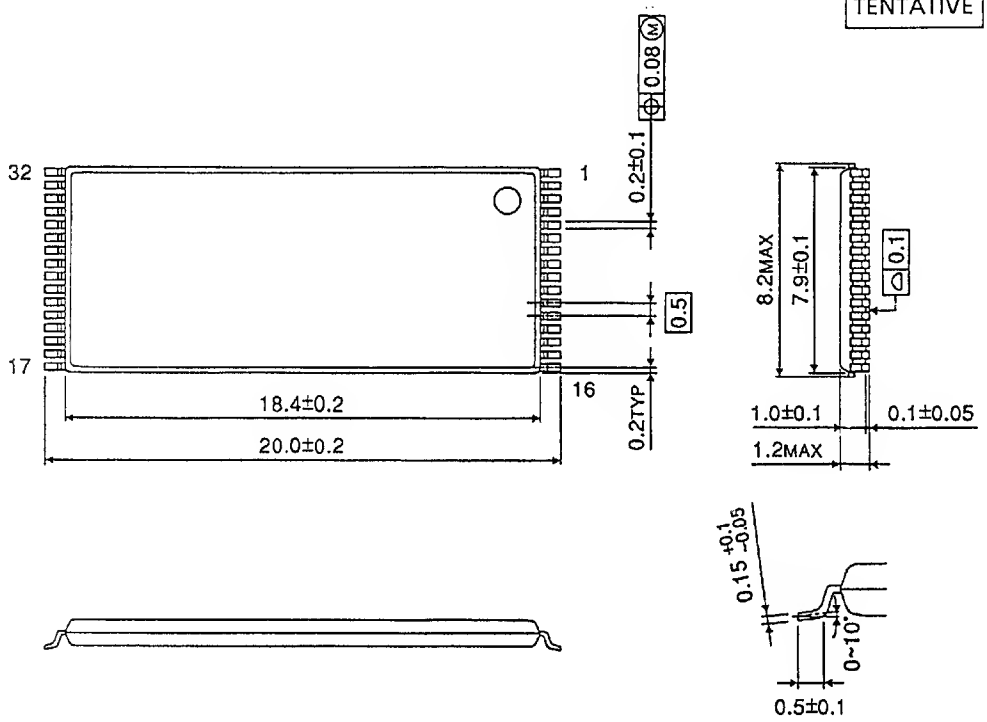
Weight : 0.36 g (Typ.)

TC518128AFTL-80
TC518128AFTL-10
TC518128AFTL-12

OUTLINE DRAWING (TSOP32 - P - 0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

TC518128ATRL-80
TC518128ATRL-10
TC518128ATRL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

PRELIMINARY

DESCRIPTION

The TC518128A-LV Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518128A-LV Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 3.135~5.5V. The $\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518128A Family has a static RAM-like write functionality where input data is written into the memory cell at the rising edge of R/W, which allows easy interfacing with microprocessor.

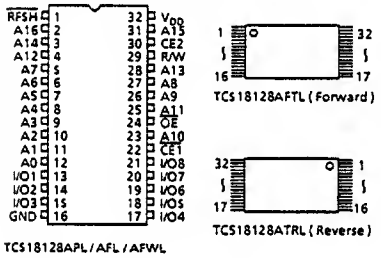
The TC518128A-LV Family is a pin-compatible with 1M bit CMOS Static RAM - JEDEC standard and is molded in a 32 pin standard 0.6 inch width plastic DIP, small-out line plastic flat package and plastic thin small-out-line package (forward, reverse type).

FEATURES

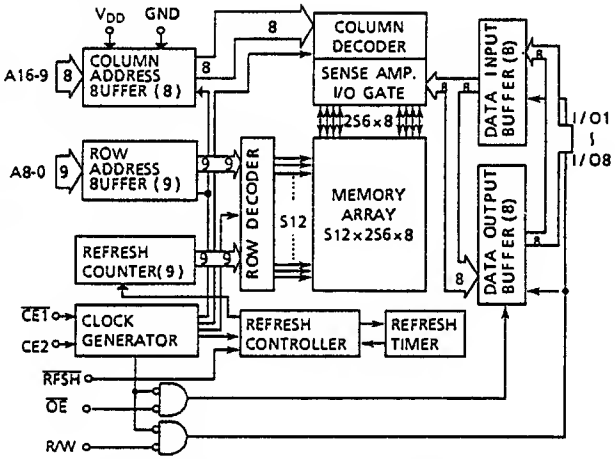
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Low Voltage Function: 3.135V~5.5V
- Data Retention Supply Voltage: 3.0V~5.5V
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs: TTL compatible
- 512 refresh cycle/8ms
- Auto refresh power down function
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- Package: TC518128APL : DIP32-P-600
  TC518128AFL : SOP32-P-450
  TC518128AFWL : SOP32-P-525
  TC518128AFTL : TSOP32-P-0820
  TC518128ATRL : TSOP32-P-0820A

		TC518128A-LV Family		
		-80	-10	-12
t_{CEA} CE Access Time		80ns	100ns	120ns
t_{OEA} OE Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ -1.0V)
* ··· Don't care (6.5V ~ -1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN ", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	-1.0~7.0	V	1
V_{OUT}	Output Voltage	-1.0~7.0	V	
V_{OO}	Power Supply Voltage	-1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	-SS~1S0	°C	
T_{SOLOER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	S0	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{OO}	Power Supply Voltage	4.S	S.0	S.S	V	2
V_{IH}	Input High Voltage	2.4	-	6.S	V	
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	80ns version	-	50	70	mA	3, 4
		100ns version	-	40	60		
		120ns version	-	35	50		
I_{DDS1}	Standby Current, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IH}		-	-	1	mA	
I_{DDS2}	Standby Current, $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = V_{DD} - 0.2V		-	100	200	μA	
I_{DDF1}	Self Refresh Current (Average Current), $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, $\overline{RFSH}$ = V_{IL}		-	-	1	mA	
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = V_{IL}		-	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		-	-	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE1}$, CE2, Address cycling : tRC = tRC min)	80ns version	-	50	70	mA	3
		100ns version	-	40	60		
		120ns version	-	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		-10	-	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}		-10	-	10	μA	
V_{OH}	Output High Level I_{OH} = -5mA		2.4	-	-	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		-	-	0.4	V	

Note) In I_{DDS1} and I_{DDF1} with $\overline{CE1}$=V_{IH}(CE2=V_{IL}), these specification limits are guaranteed under the condition of CE2=V_{IH} or CE2=V_{IL}($\overline{CE1}$=V_{IH} or $\overline{CE1}$=V_{IL}). In I_{DDS2} and I_{DDF2} with $\overline{CE1}$≧V_{DD}-0.2V(CE2≦0.2V), theses specification are guaranteed under the condition of CE2≧V_{DD}-0.2V or CE2≦0.2V($\overline{CE1}$≧V_{DD}-0.2V or $\overline{CE1}$≦0.2V).

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
C_{IO}	Input/Output Capacitance	-	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0~70°C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	CE Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from CE	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from CE	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	CE Delay Time form $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t_{CES}	CE2 Low Set-Up Time	5	-	5	-	5	-	ns	14
t_{CEH}	CE2 Low Hold Time	5	-	5	-	5	-	ns	14

[3.3V OPERATING SPECIFICATION]

D.C. RECOMMENDED OPERATING CONDITIONS (V_{DD} = 3.3V ± 5%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V	2
V_{IH}	Input High Voltage	V_{DD} - 0.2V	-	V_{DD} + 1.0V	V	
V_{IL}	Input Low Voltage	- 0.5	-	0.2	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 5%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.		-	135	200	mA	3, 4
I_{DDS2}	Standby Current		-	50	100	μA	
I_{DDF2}	Self Refresh Current (Average Current)		-	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		-	-	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE1}$, CE2, Address cycling : tRC = tRC min)		-	135	200	mA	3
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other inputs not under test = 0V		- 10	-	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, 0V ≤ V_{OUT} ≤ V_{DD}		- 10	-	10	μA	
V_{OH}	Output High Level I_{OH} = - 1mA	I_{OH} = - 1mA	2.4	-	-	V	
		I_{OH} = - 100μA	V_{DD} - 0.2V	-	-		
V_{OL}	Output Low Level I_{OL} = 2.1mA	I_{OL} = 2.1mA	-	-	0.4	V	
		I_{OL} = 100μA	-	-	0.2		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 3.3V ± 5%, Ta = 0~70 °C) (NOTES : 5, 6, 8)

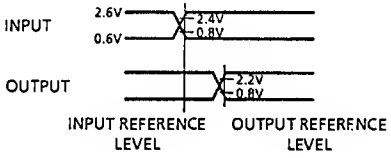
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_{RC}	Random Read, Write Cycle Time	300	-	ns	
t_{RMW}	Read Modify Write Cycle Time	405	-	ns	
t_{CE}	CE Pulse Width	200	10,000	ns	13
t_P	CE Precharge Time	90	-	ns	
t_{CEA}	CE Access Time	-	200	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	80	ns	
t_{CLZ}	CE to Output in Low-Z	40	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	-	ns	
t_{WLZ}	Output Active from End of Write	5	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	50	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	50	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	50	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	
t_{WP}	Write Pulse Width	100	-	ns	
t_{WCH}	Write Command Hold Time	100	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	100	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	50	-	ns	10
t_{DSC}	Data Set-Up Time from CE	50	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	ns	10
t_{DHC}	Data Hold Time from CE	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	ns	11
t_{AHC}	Address Hold Time	35	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	300	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	90	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	50	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	50	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	ns	12
t_{FRS}	CE Delay Time form $\overline{RFSH}$ (Self Refresh)	300	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{CES}	CE2 Low Set-Up Time	10	-	ns	14
t_{CEH}	CE2 Low Hold Time	10	-	ns	14

Timing reference Level
Input Reference Level : 1.5V / 1.5V
Output Reference Level : 1.5V / 1.5V

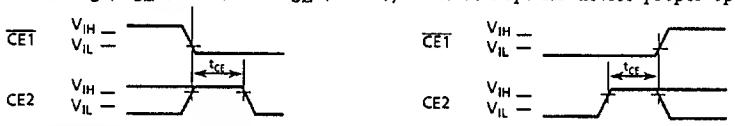
NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

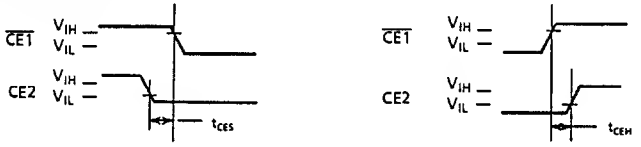
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level:		V_{OH} = 2.2V
		V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{RFSH}$ = "L" after power-up
13) The timings, t_{CE} (min.) and t_{CE} (max.), must be kept for device proper operation as follows.



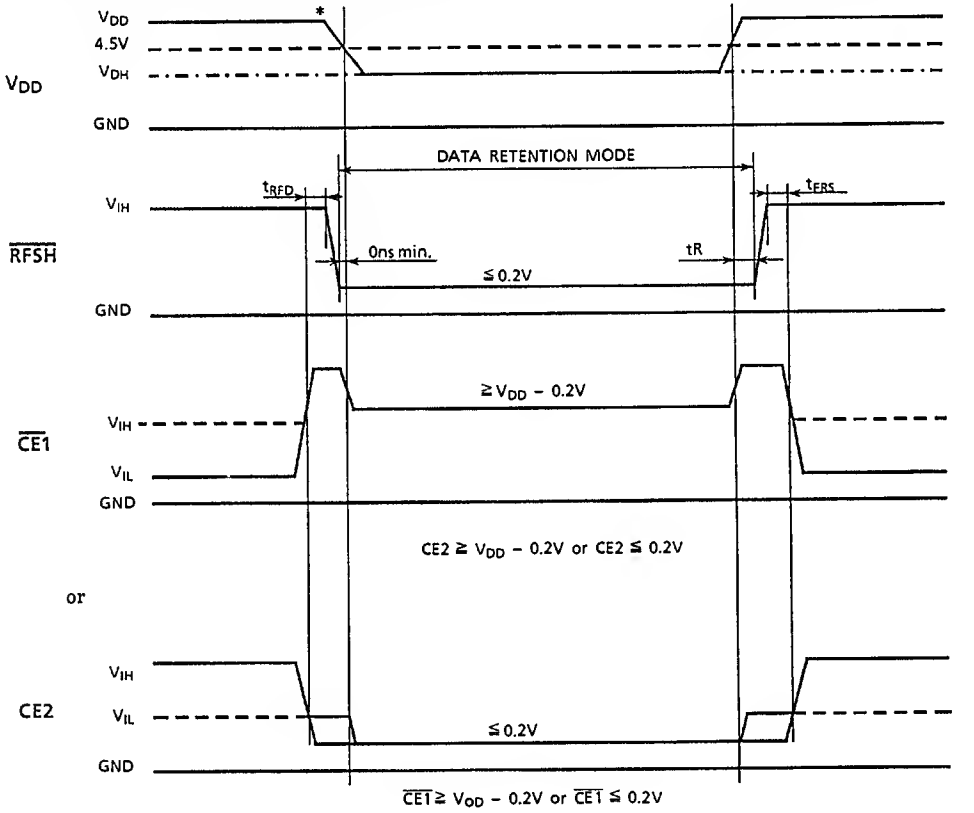
14) The timings, t_{CES} (min.) and t_{CEH} (min.), must be kept for using $\overline{CE1}$ and CE2 at the same clock as follow.



DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



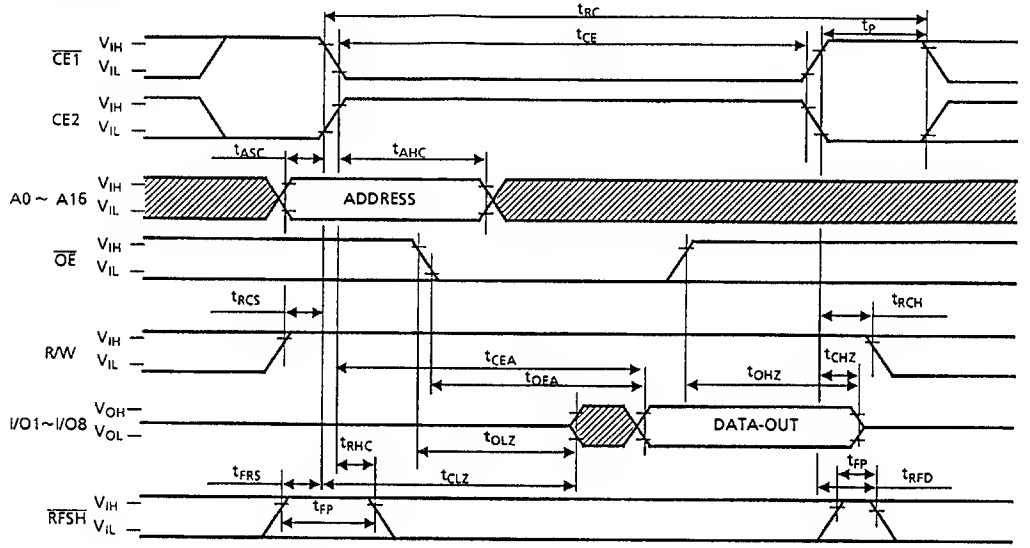
(Note) ∘ $\overline{OE}$, R/W, A0~A16 = Don't care

∘ I_{DDF1} is applied in $\overline{RFSH} = V_{IL\ max.}$, $\overline{CE1} = V_{IH\ min.}$, $CE2 = V_{IL\ max.}$

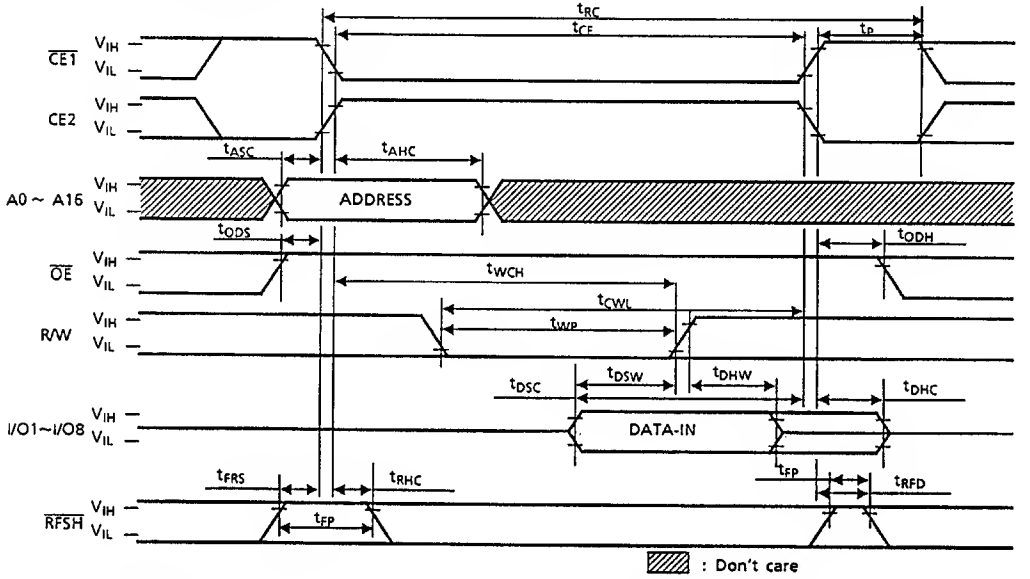
∘ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

READ CYCLE

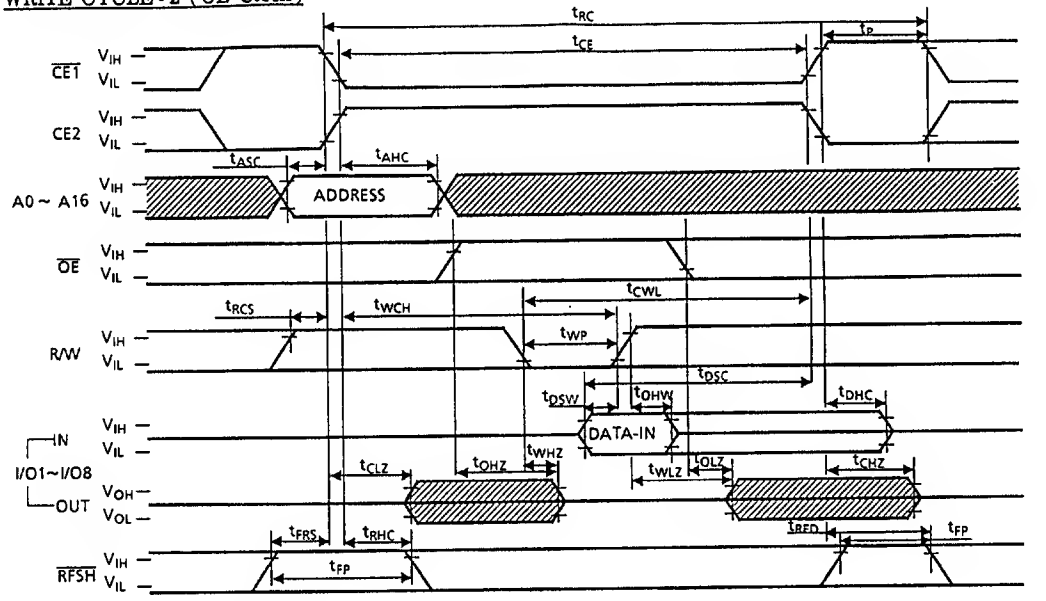


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

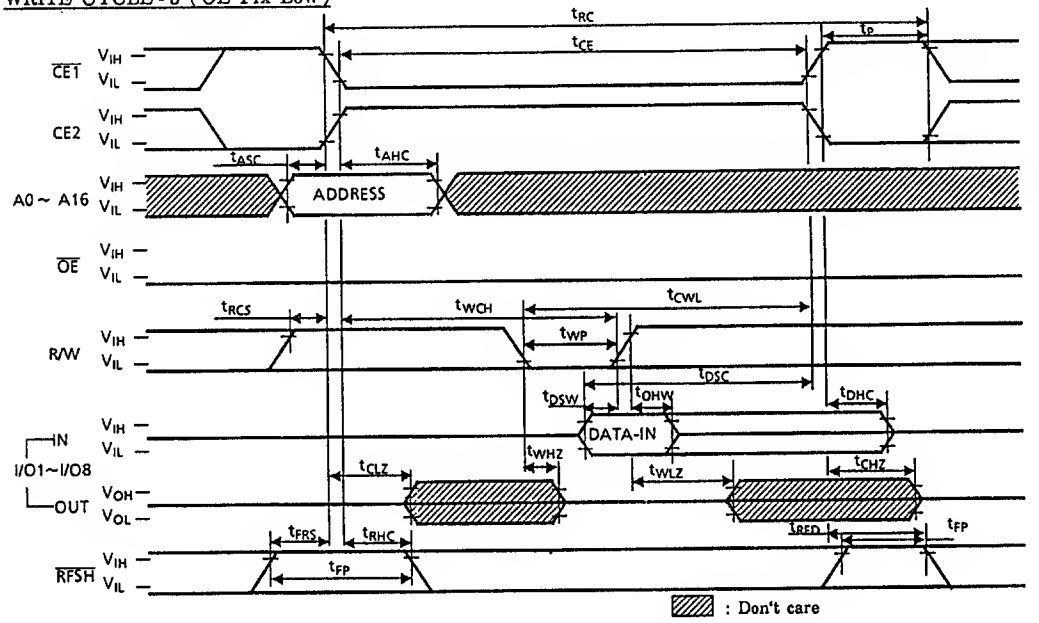


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

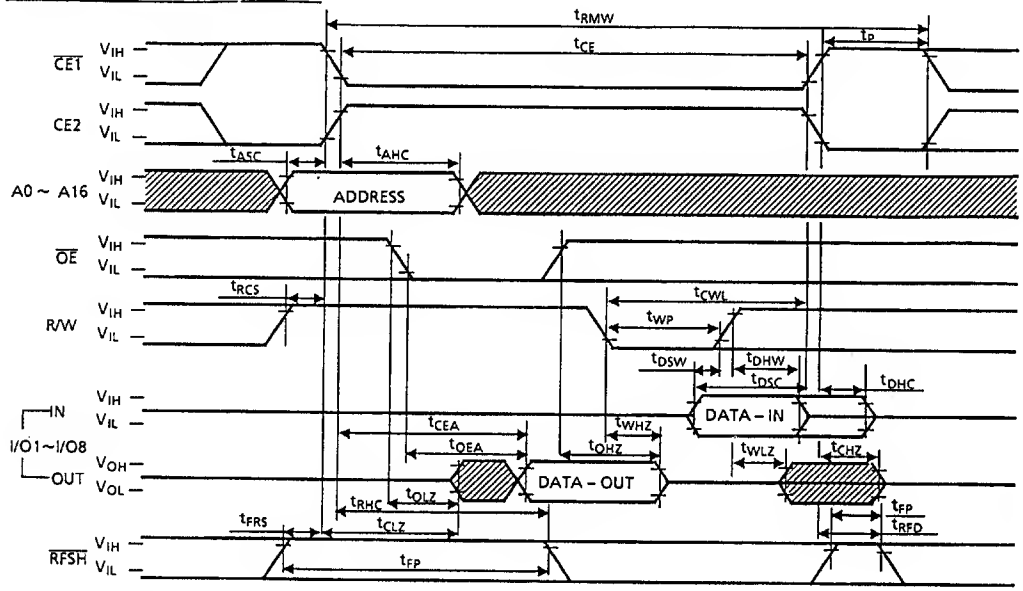


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

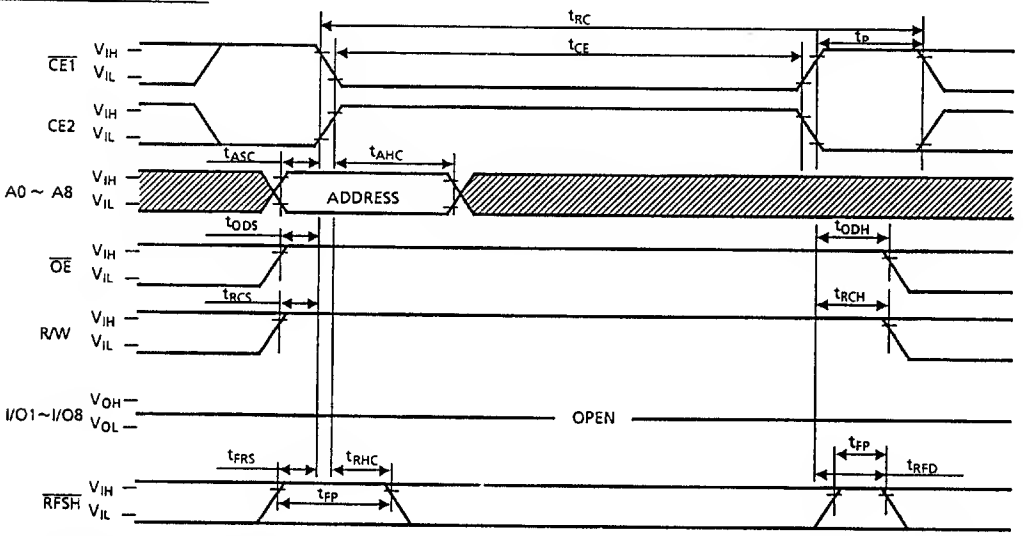


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2 "(or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

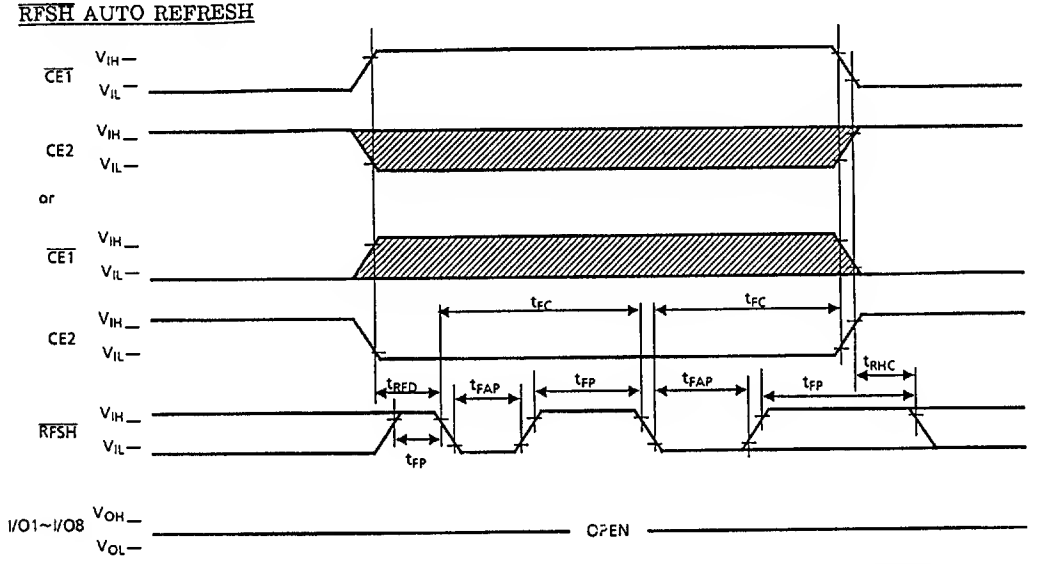


Note : A9~A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

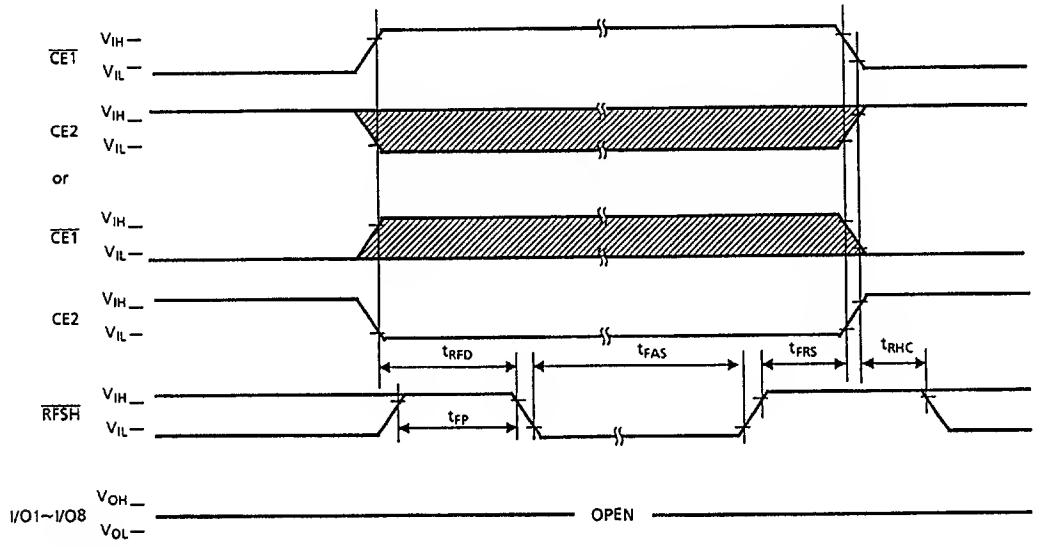
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

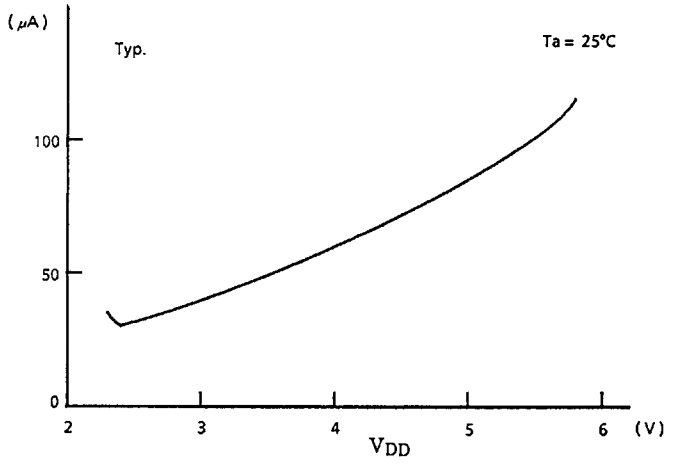
SELF REFRESH



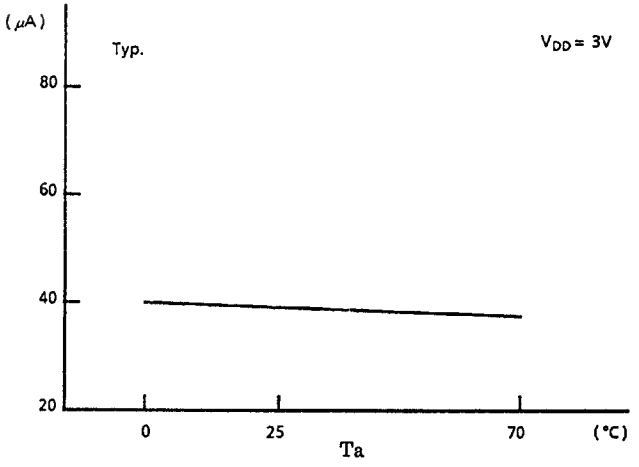
NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

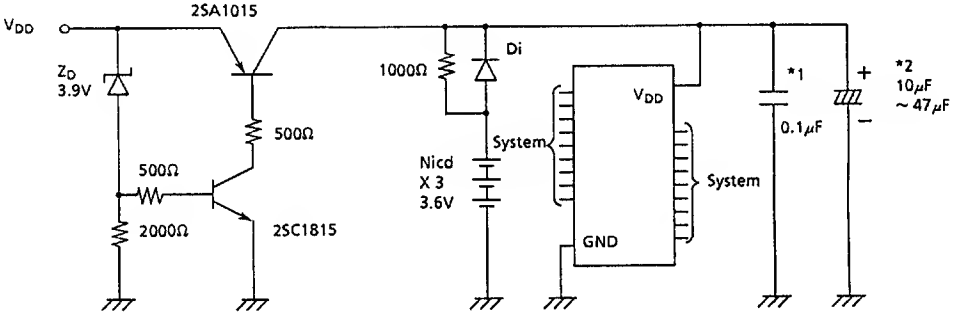
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example

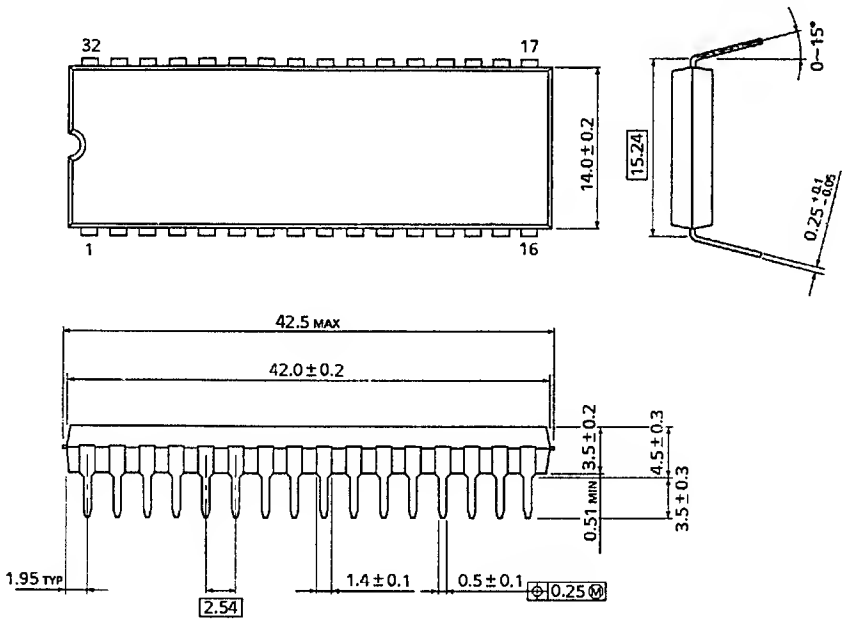


*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnning-off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWING (DIP32 - P - 600)

Unit in mm

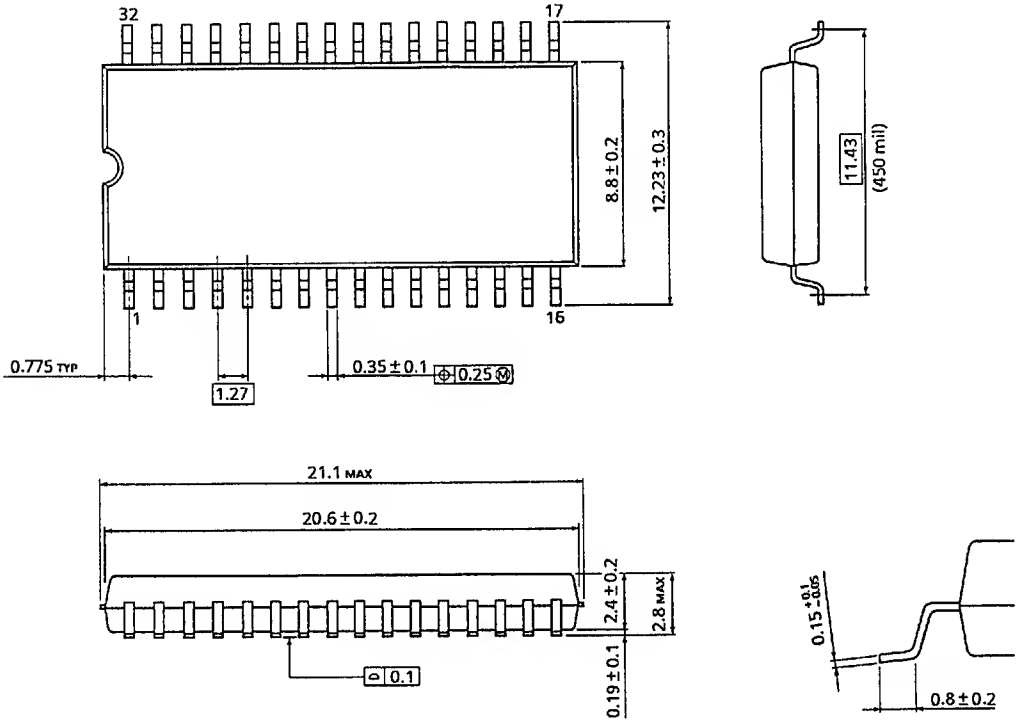


Weight : 4.53 g (Typ.)

TC518128APL-80LV
TC518128APL-10LV
TC518128APL-12LV

OUTLINE DRAWING (SOP32-P-450)

Unit in mm

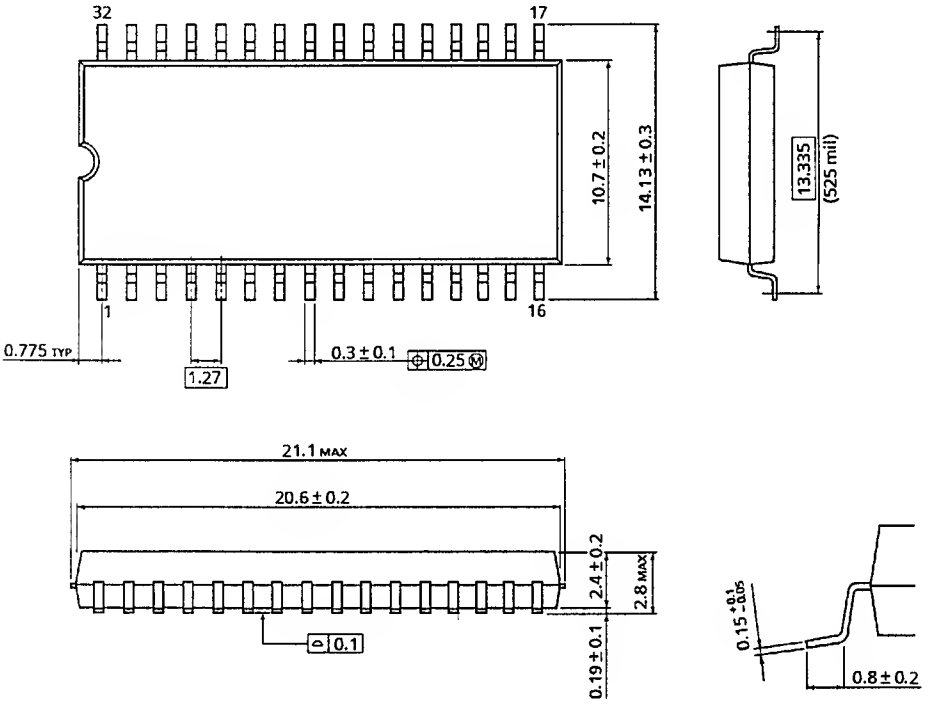


Weight : 0.87 g (Typ.)

TC518128AFL-80LV
TC518128AFL-10LV
TC518128AFL-12LV

OUTLINE DRAWING (SOP32-P-525)

Unit in mm



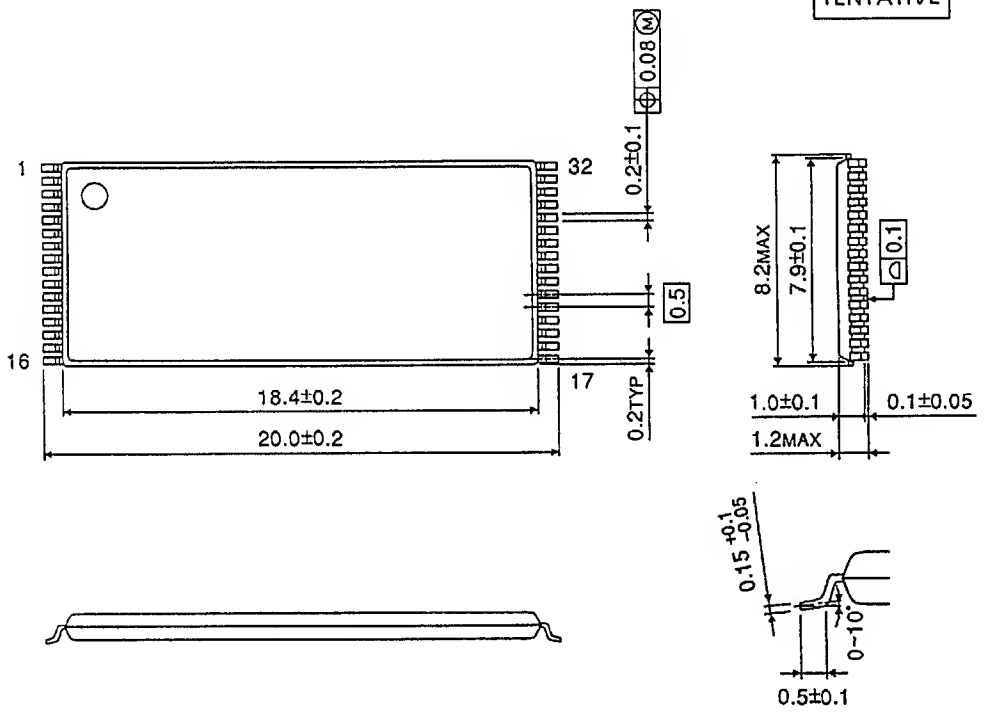
Weight : 1.10 g (Typ.)

TC518128AFWL-80LV
TC518128AFWL-10LV
TC518128AFWL-12LV

OUTLINE DRAWING (TSOP32-P-0820)

Unit in mm

TENTATIVE



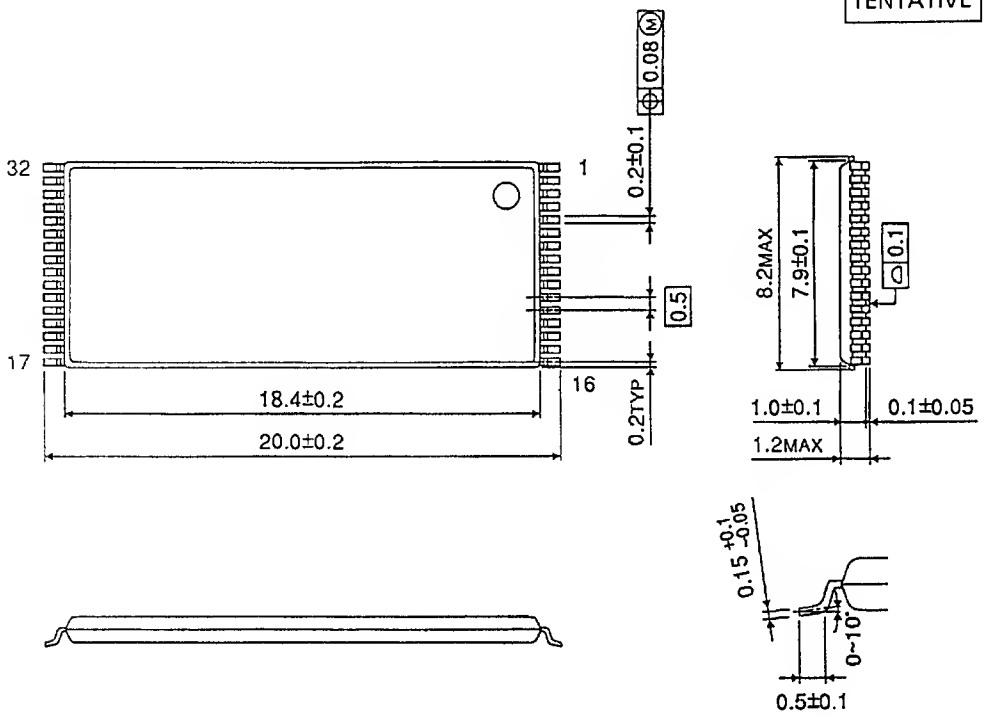
Weight : 0.36 g (Typ.)

TC518128AFTL-80LV
TC518128AFTL-10LV
TC518128AFTL-12LV

OUTLINE DRAWING (TSOP32-P-0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

TC518128ATRL-80LV
TC518128ATRL-10LV
TC518128ATRL-12LV

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518129A Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518129A Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518129A Family has a static RAM-like write functionality where input data is written into the memory cell at the rising edge of R/W, which allows easy interfacing with microprocessor.

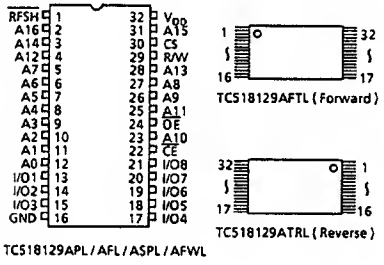
CS standby mode being adopted in the TC518129A Family, CE2 pin in the TC518128A Family is changed to CS pin. This is packaged in a 32 pin standard 0.6 inch and 0.3 inch width plastics DIP and small-out line plastic flat package and a 32 pin plastic thin small - out - line package (forward, reverse type).

FEATURES

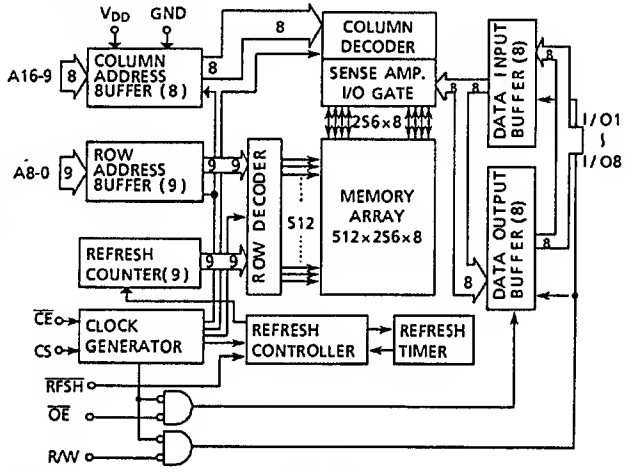
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Single Power Supply : 5V±10%
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle / 8ms
- Auto refresh power down function
- Pin Compatible : 1M SRAM (JEDEC)
- Logic Compatible : SRAM R/W Pin
- Logic Compatible : SRAM R/W Pin
- Package: TC518129AP / APL : DIP32-P-600
  TC518129AF / AFL : SOP32-P-450
  TC518129ASP/ASPL : DIP32-P-300B
  TC518129AFW/AFWL : SOP32-P-525
  TC518129AFTL : TSOP32-P-0820
  TC518129ATRL : TSOP32-P-0820A

	TC518129A Family		
	-80	-10	-12
t_{CEA} CE Access Time	80ns	100ns	120ns
t_{OEA} OE Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA / 200μA (L version)		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Inputs
CS	Chip Select Inputs
I/O1~I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CS	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}	$\overline{OE}$

FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{OO}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLOER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_O	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{OO}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3, 4
		100ns version	–	40	60		
		120ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} − 0.2V $\overline{RFSH}$ = V_{DD} − 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{DD} − 0.2V $\overline{RFSH}$ = 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE}$, Address cycling : tRC = tRC min)	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other inputs not under test = 0V		−10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		−10	–	10	μA	
V_{OH}	Output High Level I_{OH} = −5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input/Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

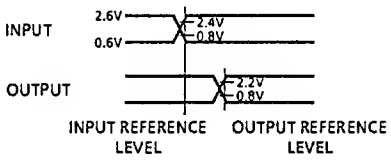
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-2	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-2	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{CSS}	Chip Select Set-Up Time	0	–	0	–	0	–	ns	
t_{CSH}	Chip Select Hold Time	20	–	25	–	30	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	$\overline{CE}$ Delay Time form $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

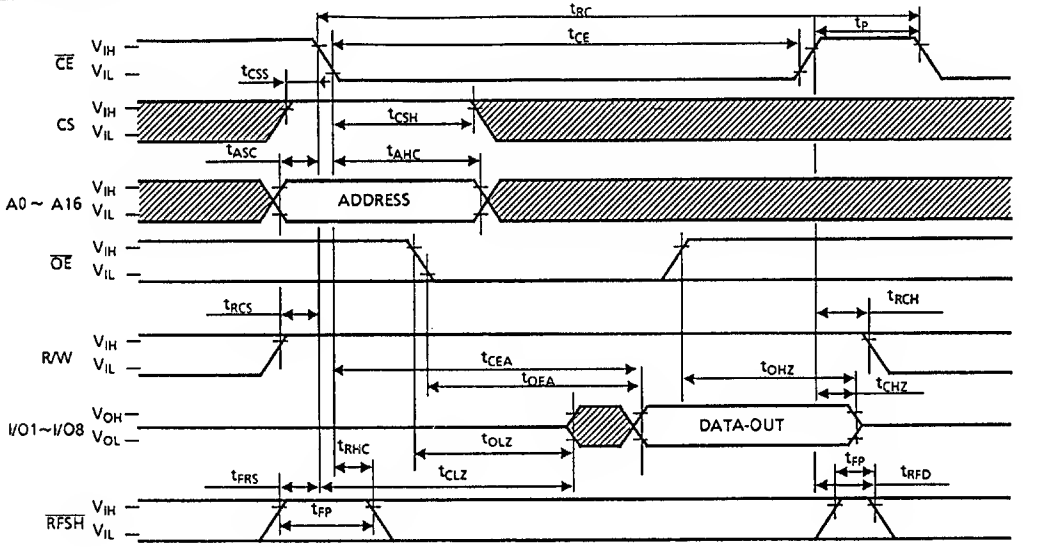
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level:		V_{OH} = 2.2V
		V_{OL} = 0.8V



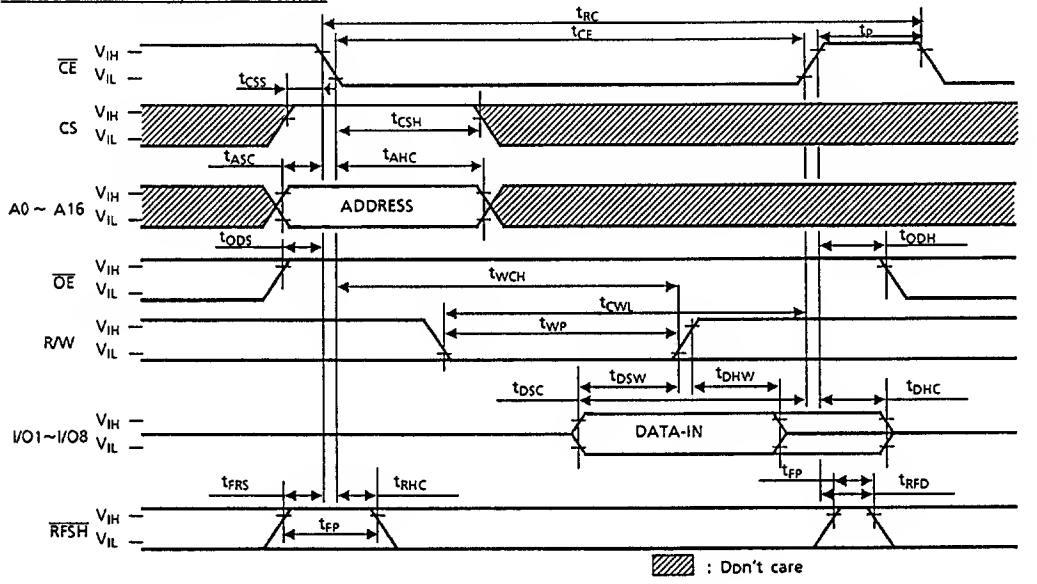
8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh : $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{RFSH}$ = "L" after power-up

TIMING WAVEFORMS

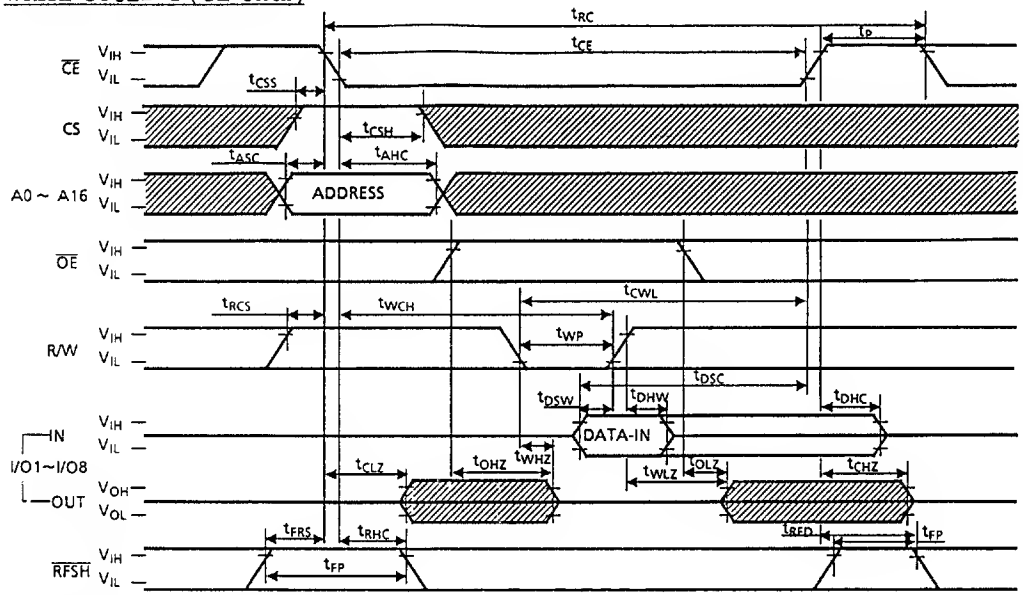
READ CYCLE



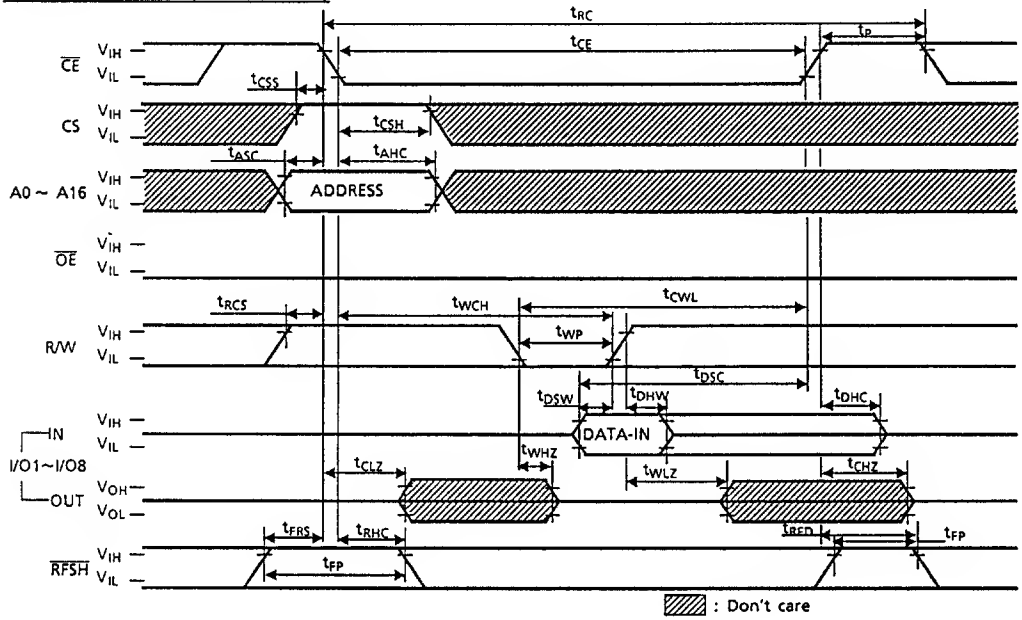
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



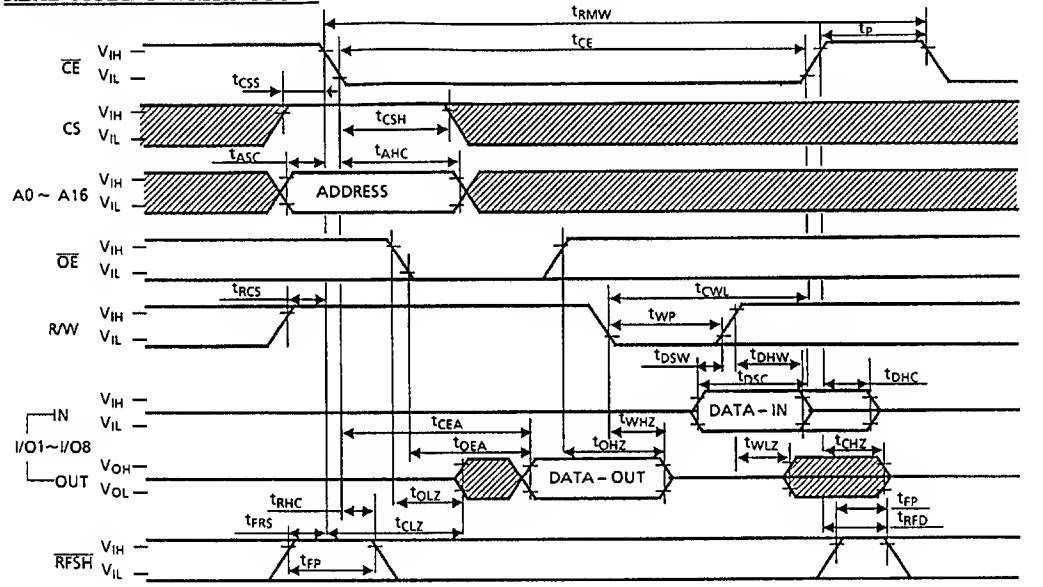
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



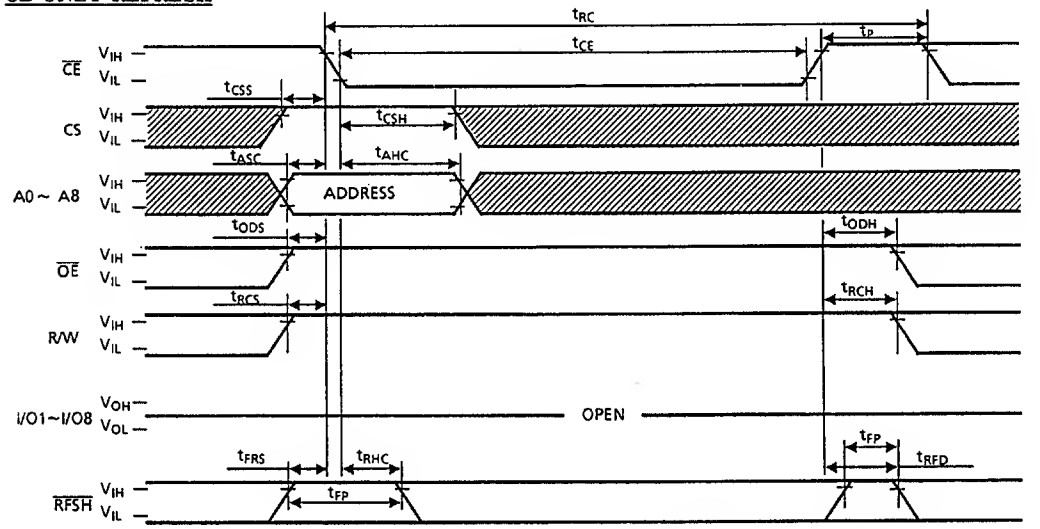
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

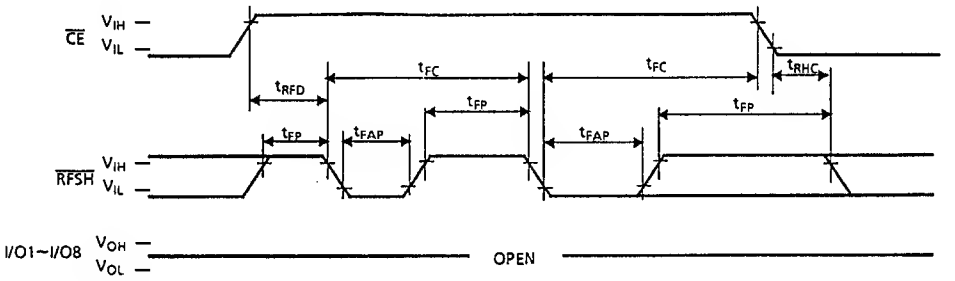


CE ONLY REFRESH



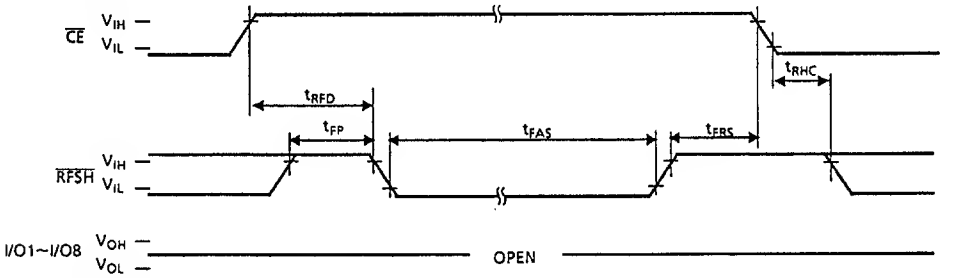
NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

$\overline{RFSH}$ AUTO REFRESH



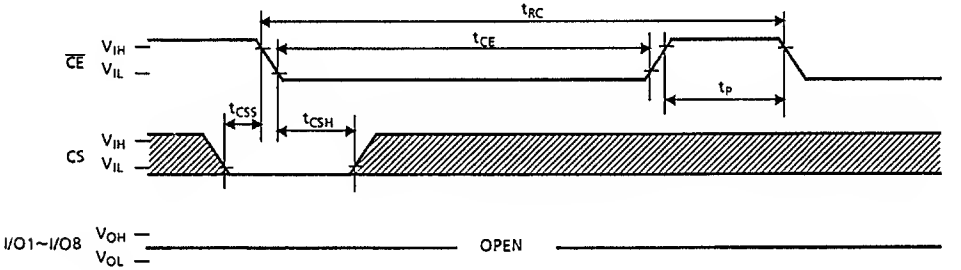
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

CS STANDBY MODE

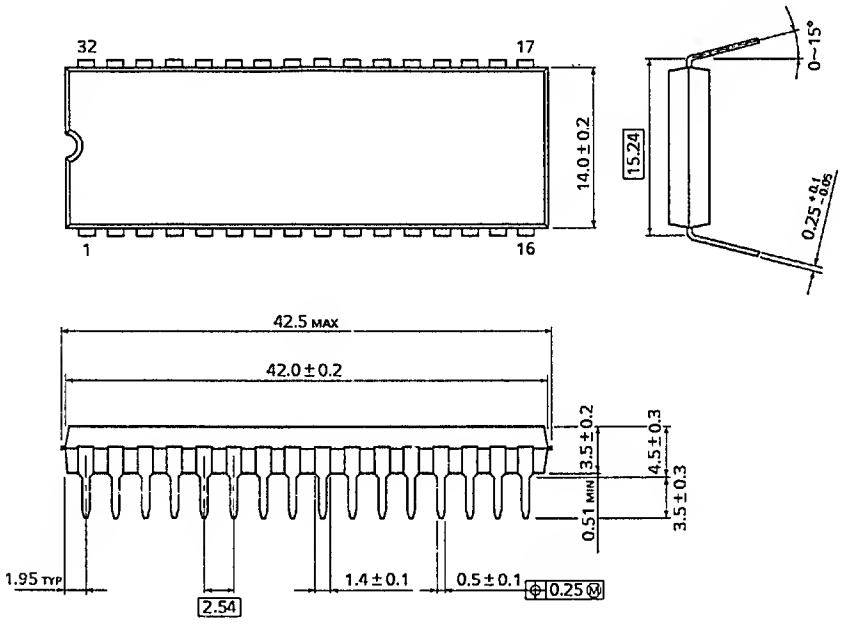


NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

OUTLINE DRAWING (DIP32 - P - 600)

Unit in mm

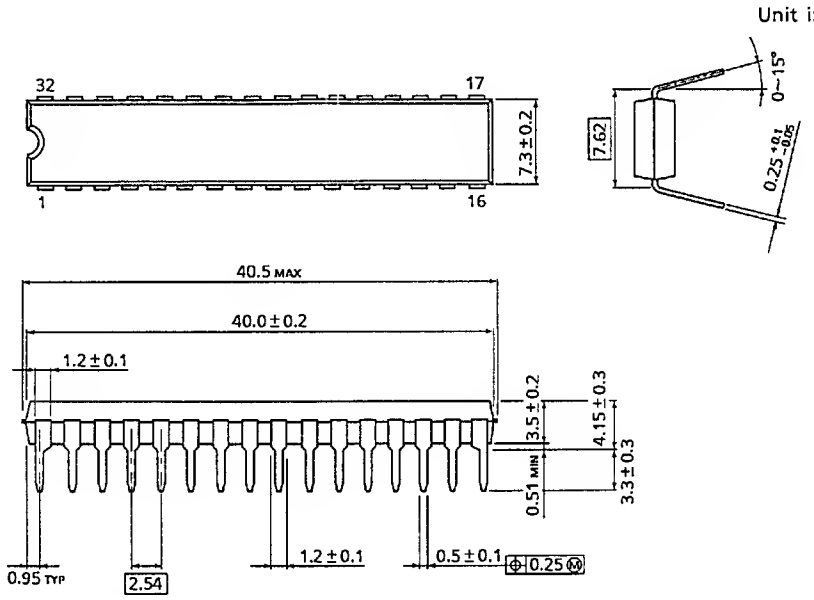


Weight : 4.53 g (Typ.)

TC518129AP-80, TC518129APL-80
TC518129AP-10, TC518129APL-10
TC518129AP-12, TC518129APL-12

OUTLINE DRAWING (DIP32 - P - 300)

Unit in mm

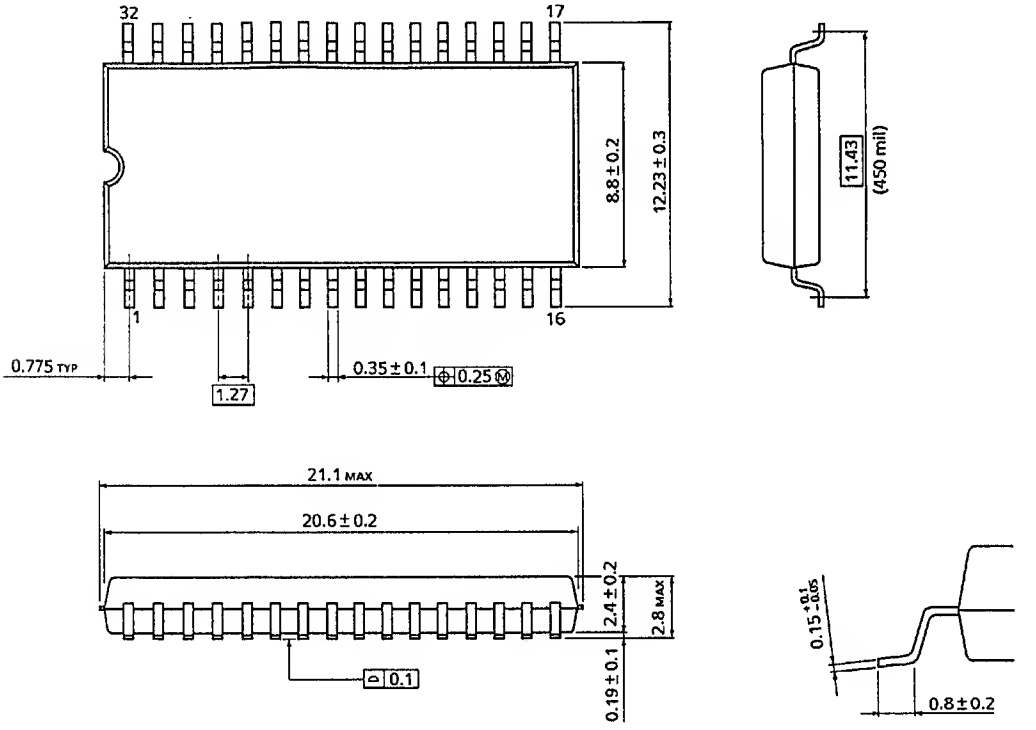


Weight : 2.36 g (Typ.)

TC518129ASP-80, TC518129ASPL-80
TC518129ASP-10, TC518129ASPL-10
TC518129ASP-12, TC518129ASPL-12

OUTLINE DRAWING (SOP32 - P - 450)

Unit in mm

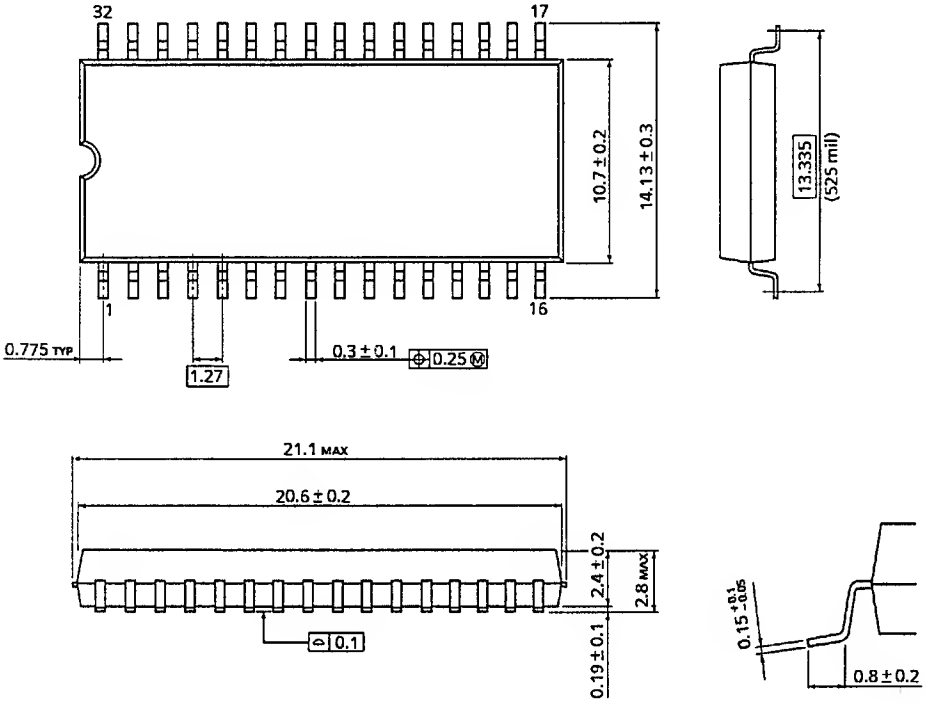


Weight : 0.87 g (Typ.)

TC518129AF-80, TC518129AFL-80
TC518129AF-10, TC518129AFL-10
TC518129AF-12, TC518129AFL-12

OUTLINE DRAWING (SOP32 – P – 525)

Unit in mm



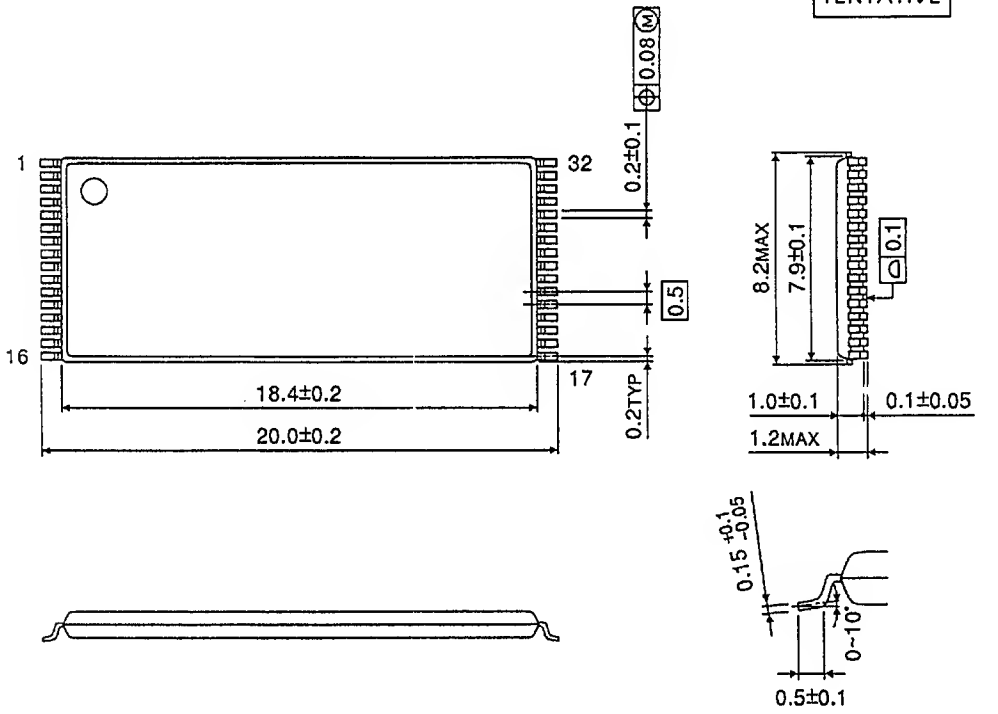
Weight : 1.10 g (Typ.)

TC518129AFW-80, TC518129AFWL-80
TC518129AFW-10, TC518129AFWL-10
TC518129AFW-12, TC518129AFWL-12

OUTLINE DRAWING (TSOP32 - P - 0820)

Unit in mm

TENTATIVE



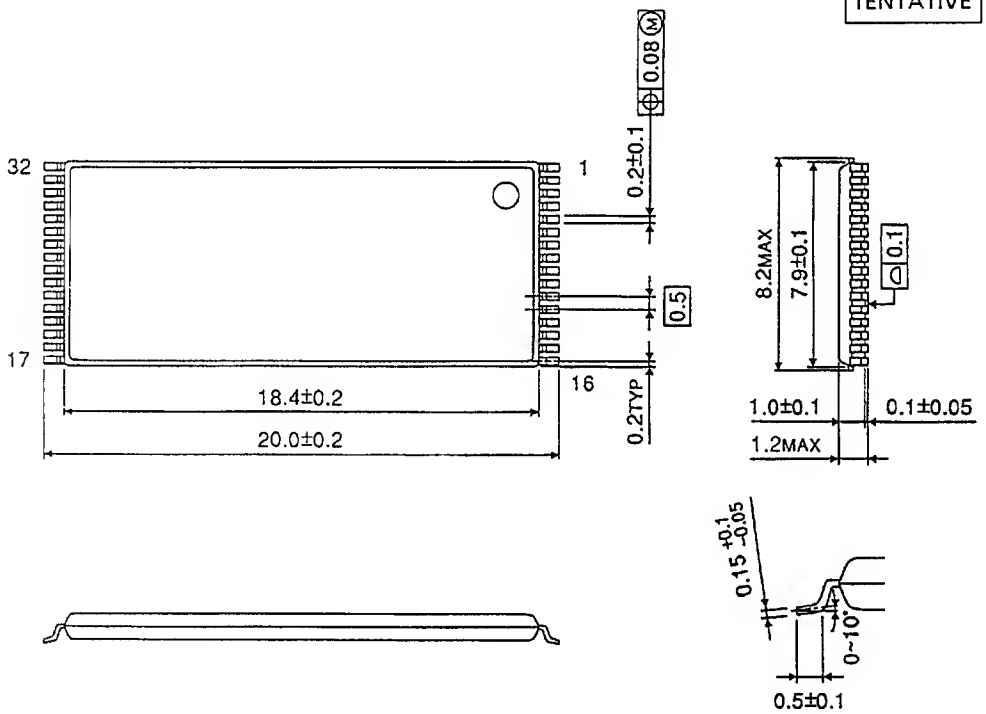
Weight : 0.36 g (Typ.)

TC518129AFTL-80
TC518129AFTL-10
TC518129AFTL-12

OUTLINE DRAWING (TSOP32 - P - 0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

TC518129ATRL-80
TC518129ATRL-10
TC518129ATRL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

PRELIMINARY

DESCRIPTION

The TC518129A-LV Family is a 1M bit high speed CMOS Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518129A-LV Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 3.135V~5.5V. The $\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518129A-LV Family has a static RAM-like write functionality where input data is written into the memory cell at the rising edge of R/W, which allows easy interfacing with microprocessor.

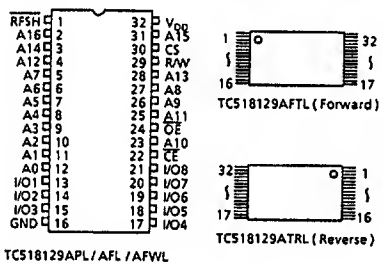
CS standby mode being adopted in the TC518129A-LV Family, CE2 pin in the TC518128A Family is changed to CS pin. This is packaged in a 32 pin standard 0.6 inch width plastics DIP, small-out line plastic flat package and plastic thin small-out-line package (forward, reverse type).

FEATURES

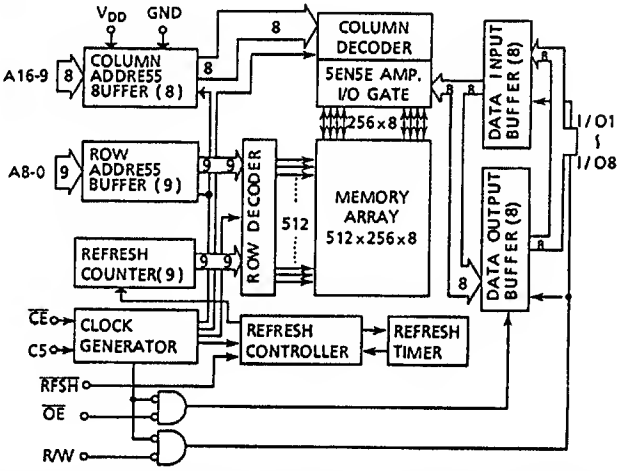
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation
- Low Voltage Function: 3.135V~5.5V
- Data Retention Supply Voltage: 3.0V~5.5V
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs: TTL compatible
- CS standby cycle is capable
- 512 refresh cycle/8ms
- Auto refresh power down function
- Logic Compatible: SRAM R/W Pin
- Package: TC518129APL : DIP32-P-600
  TC518129AFL : SOP32-P-450
  TC518129AFWL : SOP32-P-525
  TC518129AFTL : TSOP32-P-0820
  TC518129ATRL : TSOP32-P-0820A

		TC518129A-LV Family		
		-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time		80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Inputs
CS	Chip Select Inputs
I/O1~I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CS	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}	$\overline{OE}$

FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	*	V*	OUT	Read
L	H	*	L	*	V*	IN	Write
L	H	H	H	*	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ -1.0V)
* ··· Don't care (6.5V ~ -1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	-1.0~7.0	V	1
V_{OUT}	Output Voltage	-1.0~7.0	V	
V_{DD}	Power Supply Voltage	-1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	-55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS	NOTE
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3, 4
		100ns version	–	40	60		
		120ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} – 0.2V, $\overline{RFSH}$ = V_{DD} – 0.2V		–	100	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{DD} – 0.2V, $\overline{RFSH}$ = 0.2V		–	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE}$, Address cycling : tRC = tRC min)	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V		–10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		–10	–	10	μA	
V_{OH}	Output High Level I_{OH} = –5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input/Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{CSS}	Chip Select Set-Up Time	0	-	0	-	0	-	ns	
t_{CSH}	Chip Select Hold Time	20	-	25	-	30	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	$\overline{CE}$ Delay Time form $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

[3.3V OPERATING SPECIFICATION]

D.C. RECOMMENDED OPERATING CONDITIONS (V_{DD} = 3.3V ± 5%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V	2
V_{IH}	Input High Voltage	V_{DD} - 0.2V	-	V_{DD} + 1.0V	V	
V_{IL}	Input Low Voltage	-0.5	-	0.2	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 5%, Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$ Address cycling: t_{RC} = t_{RC} min.		-	15	20	mA	3, 4
I_{DDS2}	Standby Current		-	50	100	μA	
I_{DDF2}	Self Refresh Current (Average Current)		-	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{RFSH}$ cycling : tFC = tFC min)		-	-	2	mA	
I_{DDF4}	CE only Refresh Current (Average Current) ($\overline{CE}$ Address cycling : tRC = tRC min)		-	15	20	mA	3
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		-10	-	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, 0V ≤ V_{OUT} ≤ V_{DD}		-10	-	10	μA	
V_{OH}	Output High Level I_{OH} = -1mA	I_{OH} = -1mA	2.4	-	-	V	
		I_{OH} = -100μA	V_{DD} - 0.2V	-	-		
V_{OL}	Output Low Level I_{OL} = 2.1mA	I_{OL} = 2.1mA	-	-	0.4	V	
		I_{OL} = 100μA	-	-	0.2		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 3.3V ± 5%, Ta = 0~70 °C) (NOTES : 5, 6, 8)

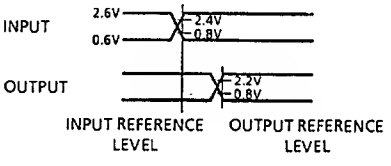
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_{RC}	Random Read, Write Cycle Time	300	-	ns	
t_{RMW}	Read Modify Write Cycle Time	405	-	ns	
t_{CE}	CE Pulse Width	200	10,000	ns	
t_{P}	CE Precharge Time	90	-	ns	
t_{CEA}	CE Access Time	-	200	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	80	ns	
t_{CLZ}	CE to Output in Low-Z	40	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	-	ns	
t_{WLZ}	Output Active from End of Write	5	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	50	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	50	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	50	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	
t_{WP}	Write Pulse Width	100	-	ns	
t_{WCH}	Write Command Hold Time	100	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	100	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	50	-	ns	10
t_{DSC}	Data Set-Up Time from CE	50	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	ns	10
t_{DHC}	Data Hold Time from CE	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	ns	11
t_{AHC}	Address Hold Time	35	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	300	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	90	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	50	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	50	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	ns	12
t_{FRS}	CE Delay Time form $\overline{RFSH}$ (Self Refresh)	300	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	ms	
t_{T}	Transition Time (Rise and Fall)	3	50	ns	

Timing reference Level
Input Reference Level : 1.5V / 1.5V
Output Reference Level : 1.5V / 1.5V

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V

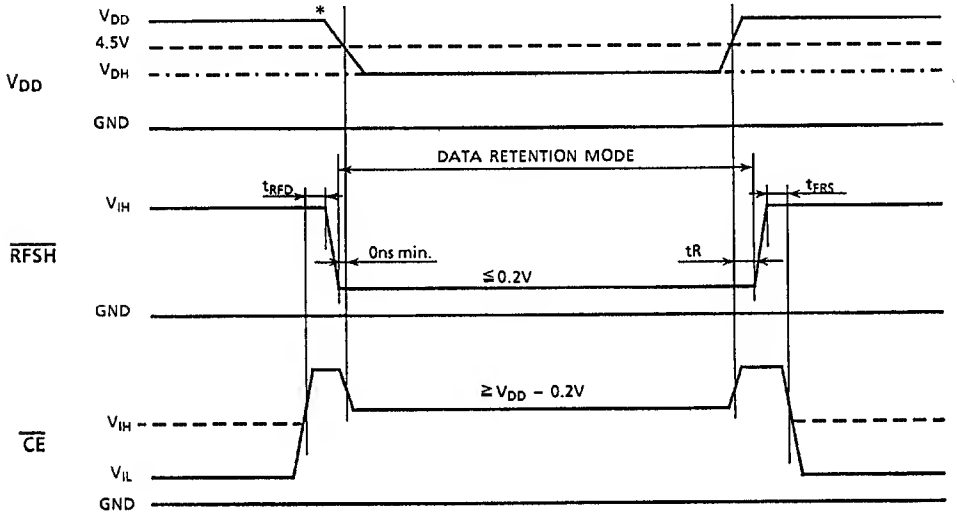


8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{RFSH}$ = "L" after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



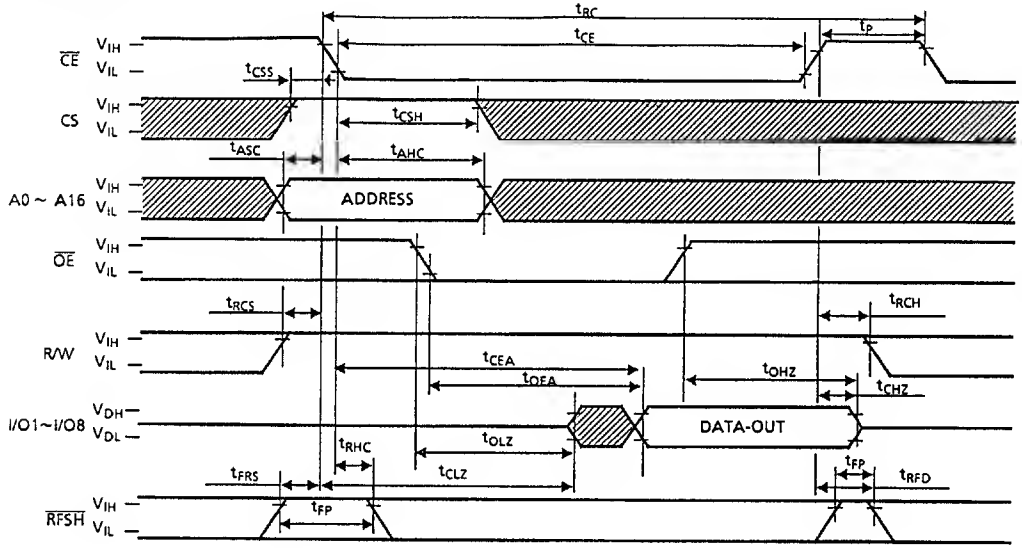
(Note) ◦ CS, $\overline{OE}$, R/W, A0~A16 = Don't care

◦ I_{DDF1} is applied in $\overline{RFSH}$ = V_{IL} max., $\overline{CE}$ = V_{IH} min.

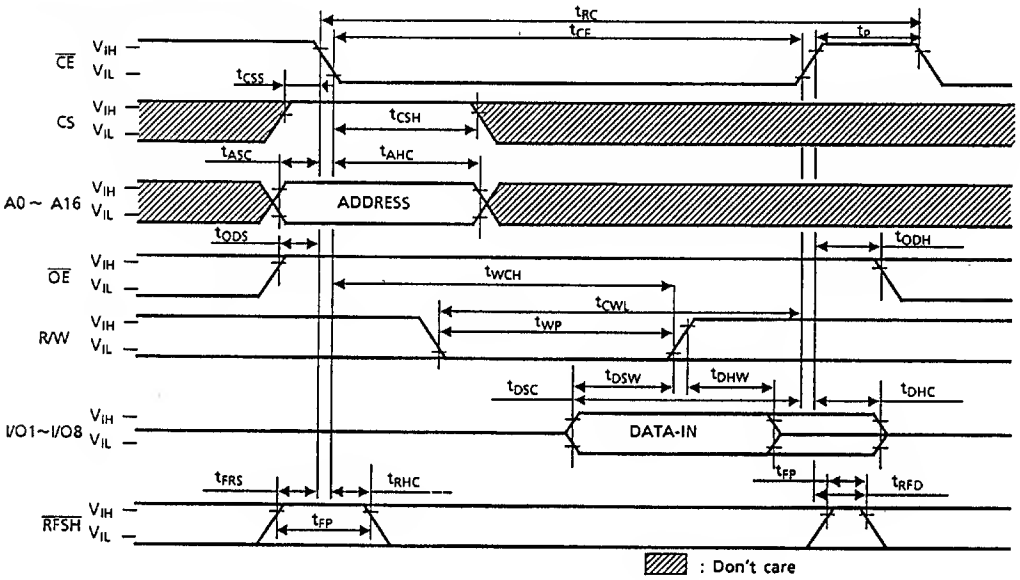
◦ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

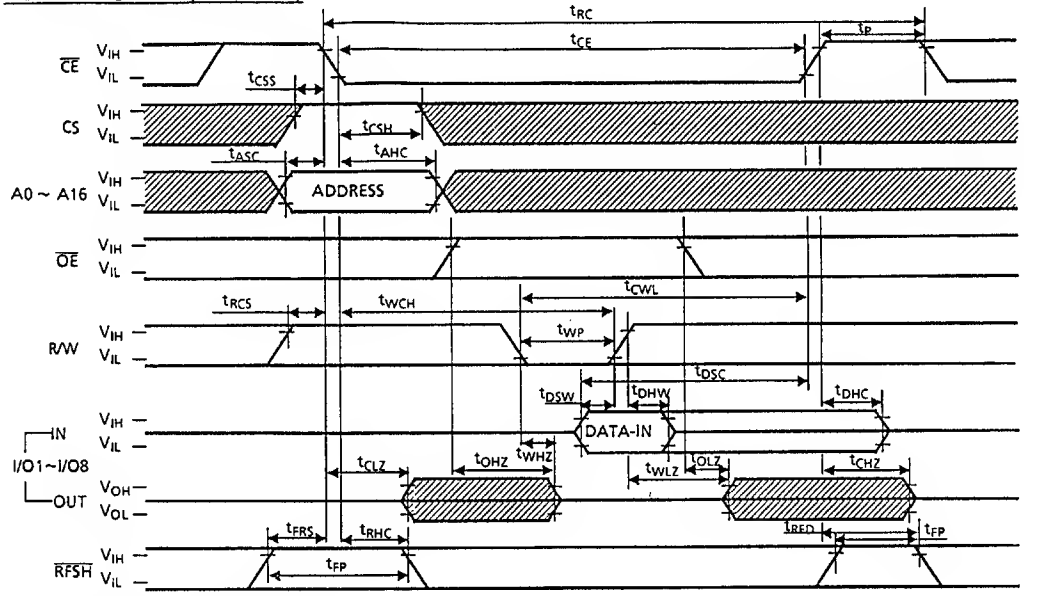
READ CYCLE



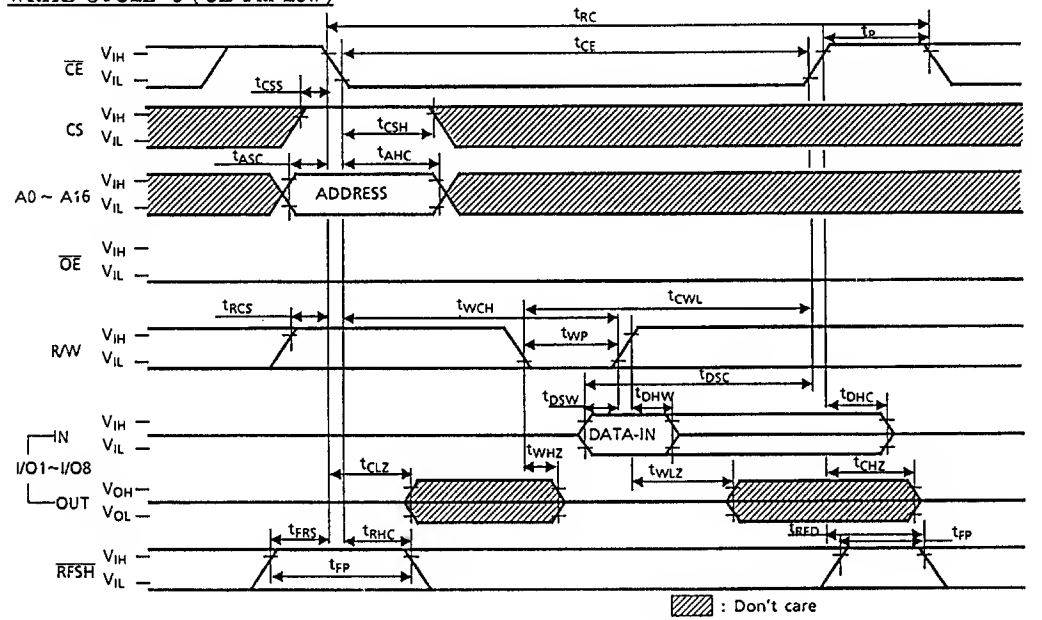
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



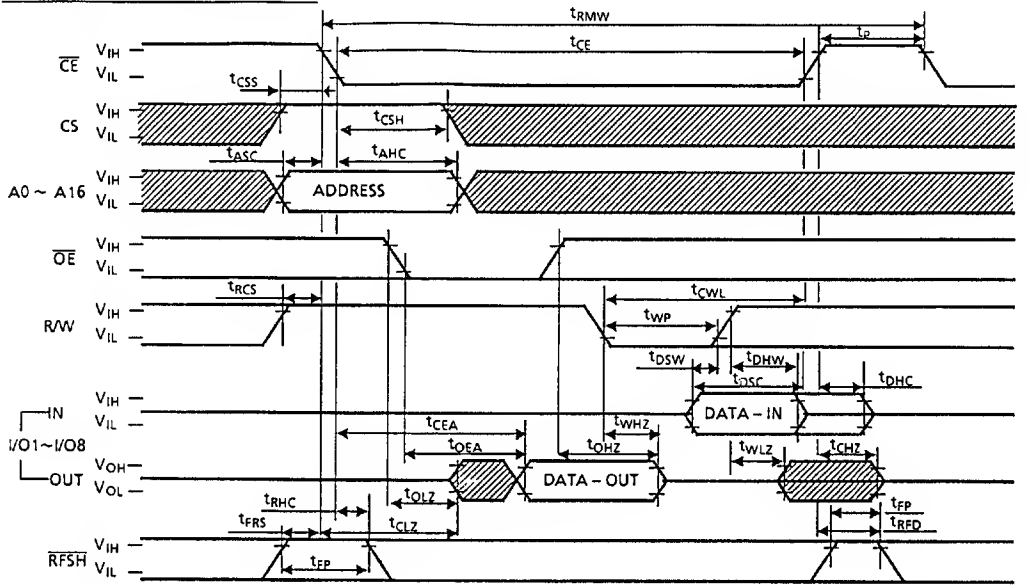
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



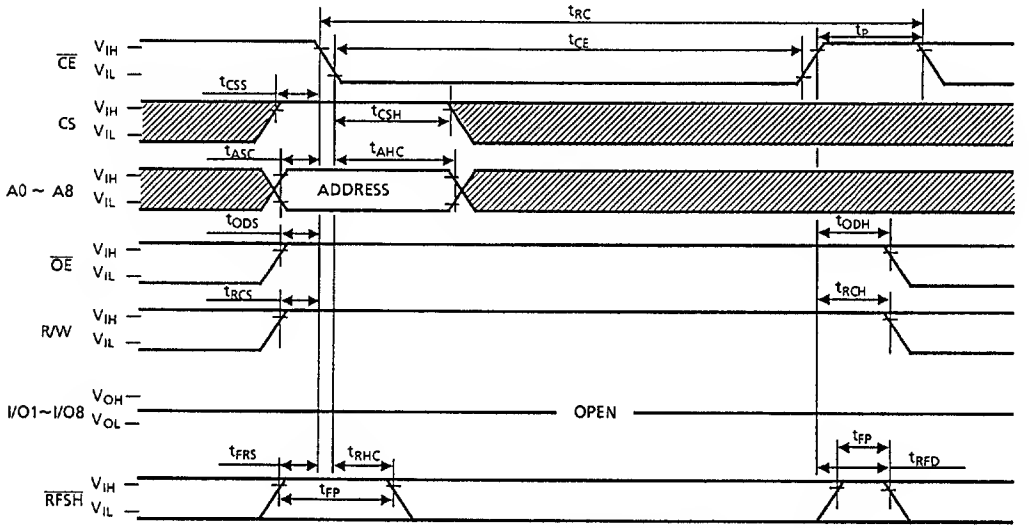
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

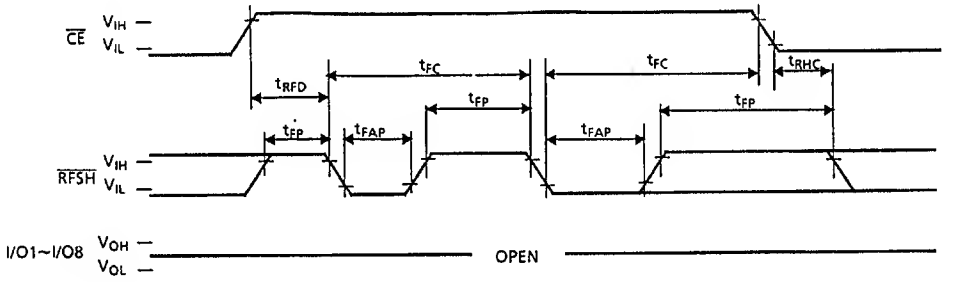


CE ONLY REFRESH



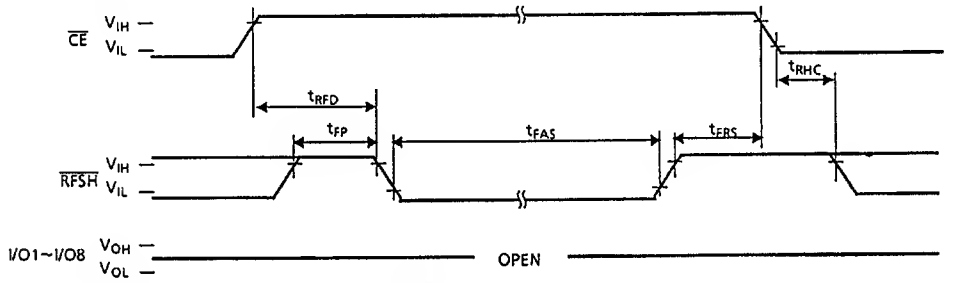
NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

$\overline{RFSH}$ AUTO REFRESH



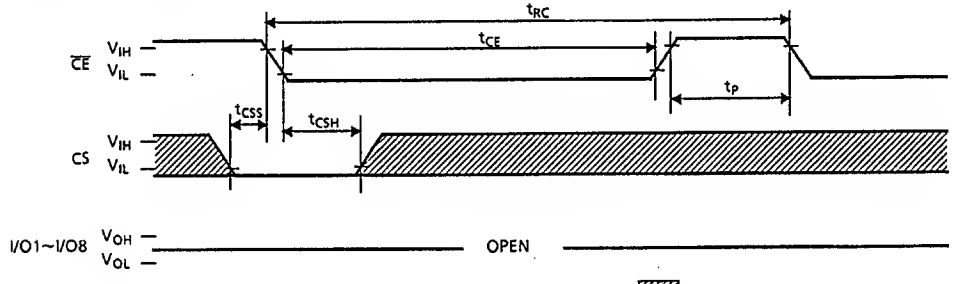
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

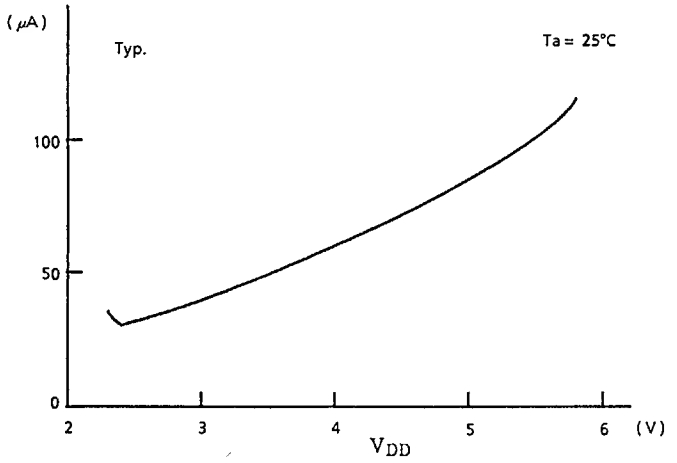
CS STANDBY MODE



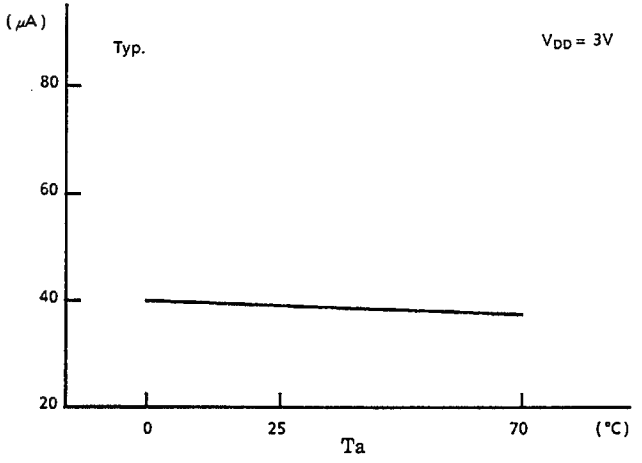
NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

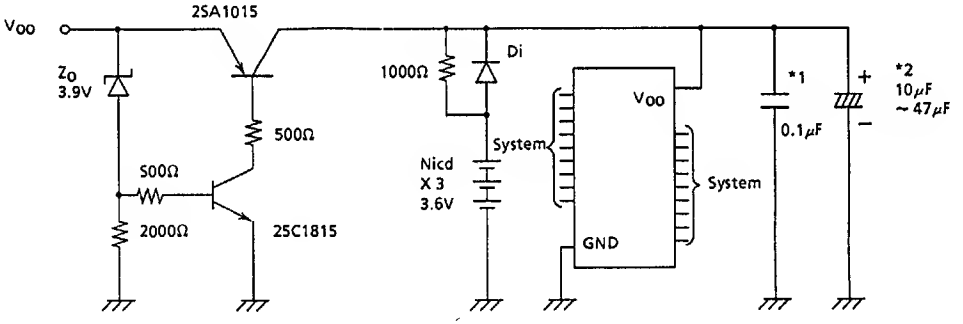
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example

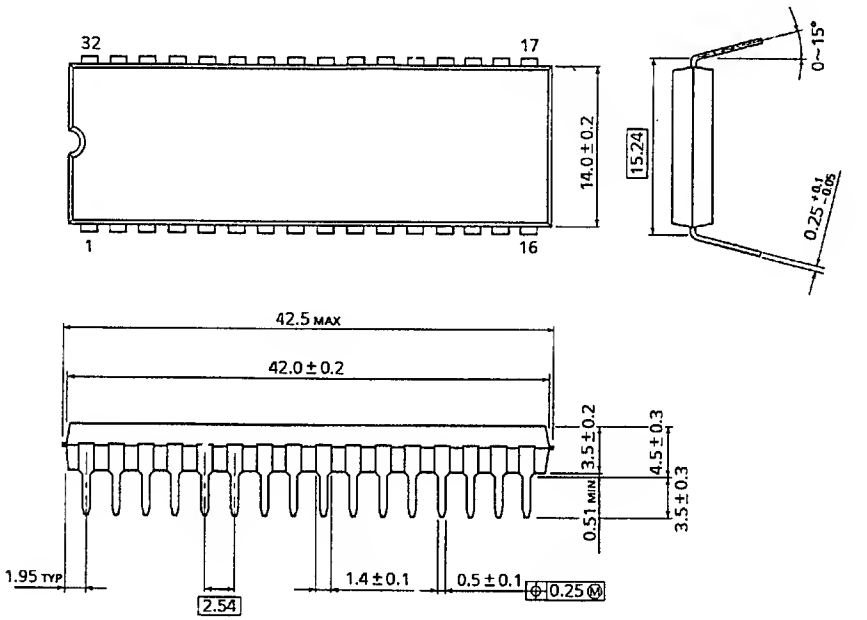


*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnning-off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWING (DIP32 - P - 600)

Unit in mm

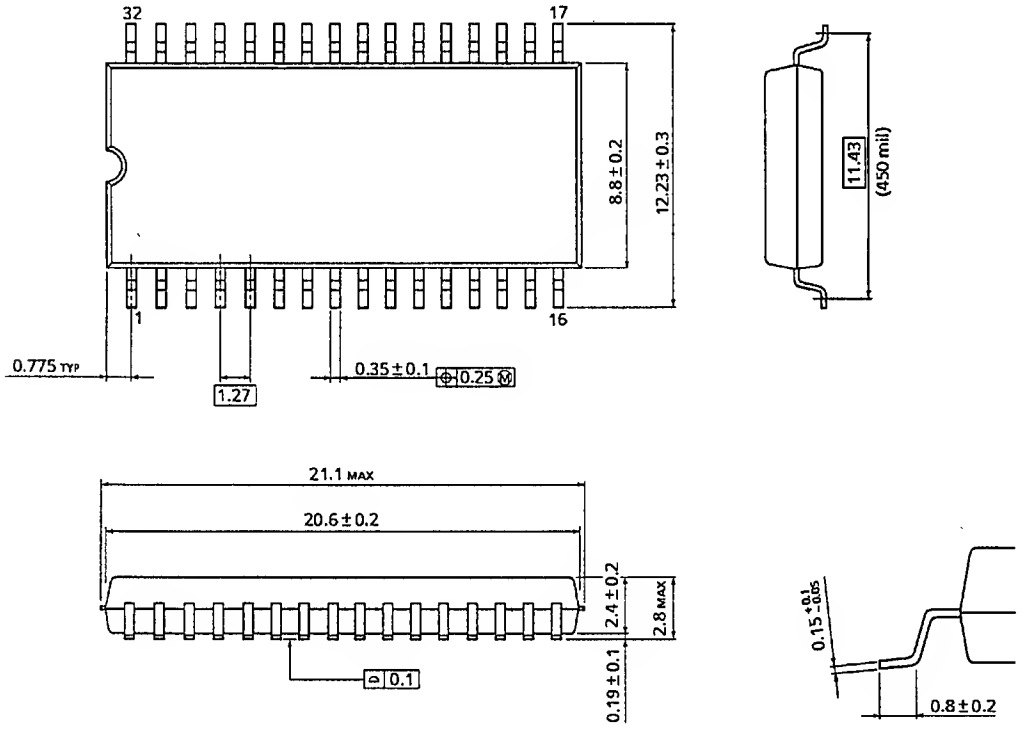


Weight : 4.53 g (Typ.)

TC518129APL-80LV
TC518129APL-10LV
TC518129APL-12LV

OUTLINE DRAWING (SOP32-P-450)

Unit in mm

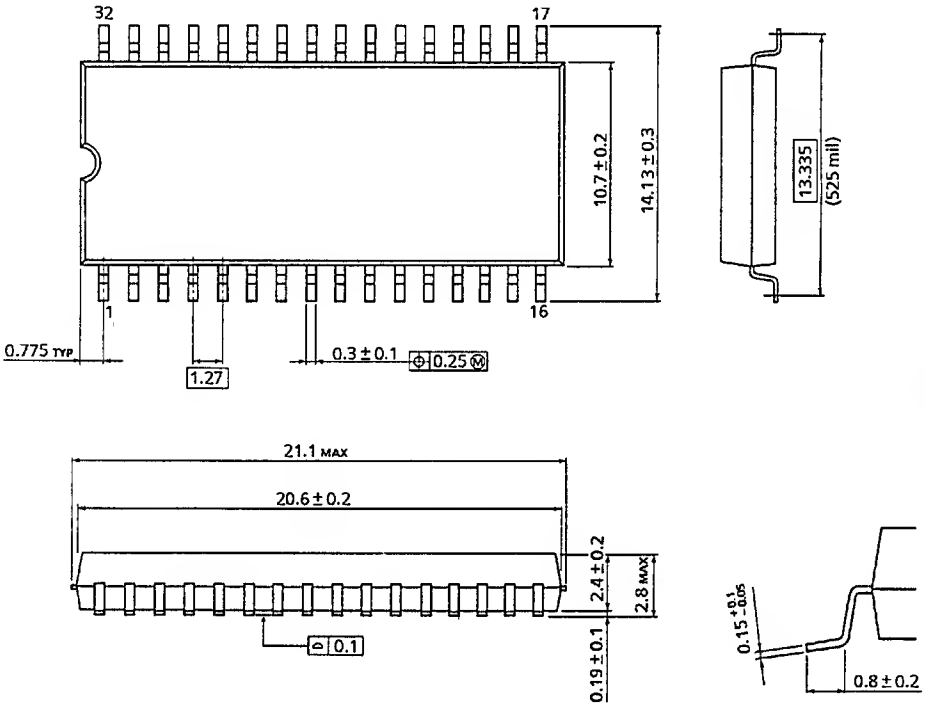


Weight : 0.87 g (Typ.)

TC518129AFL-80LV
TC518129AFL-10LV
TC518129AFL-12LV

OUTLINE DRAWING (SOP32-P-525)

Unit in mm



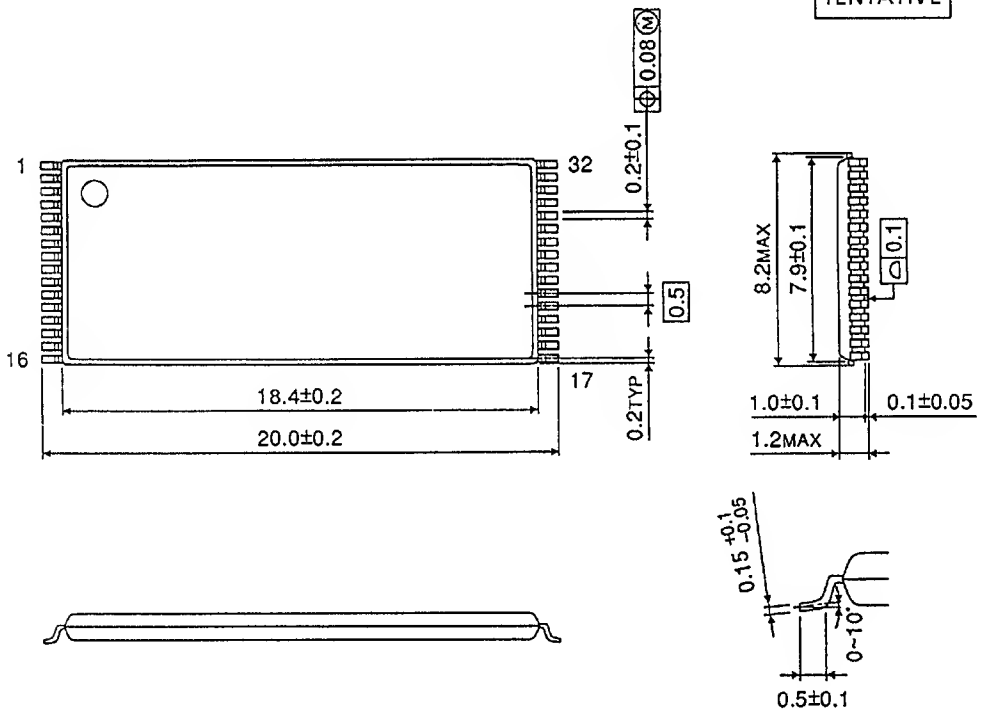
Weight : 1.10 g (Typ.)

TC518129AFWL-80LV
TC518129AFWL-10LV
TC518129AFWL-12LV

OUTLINE DRAWING (TSOP32-P-0820)

Unit in mm

TENTATIVE



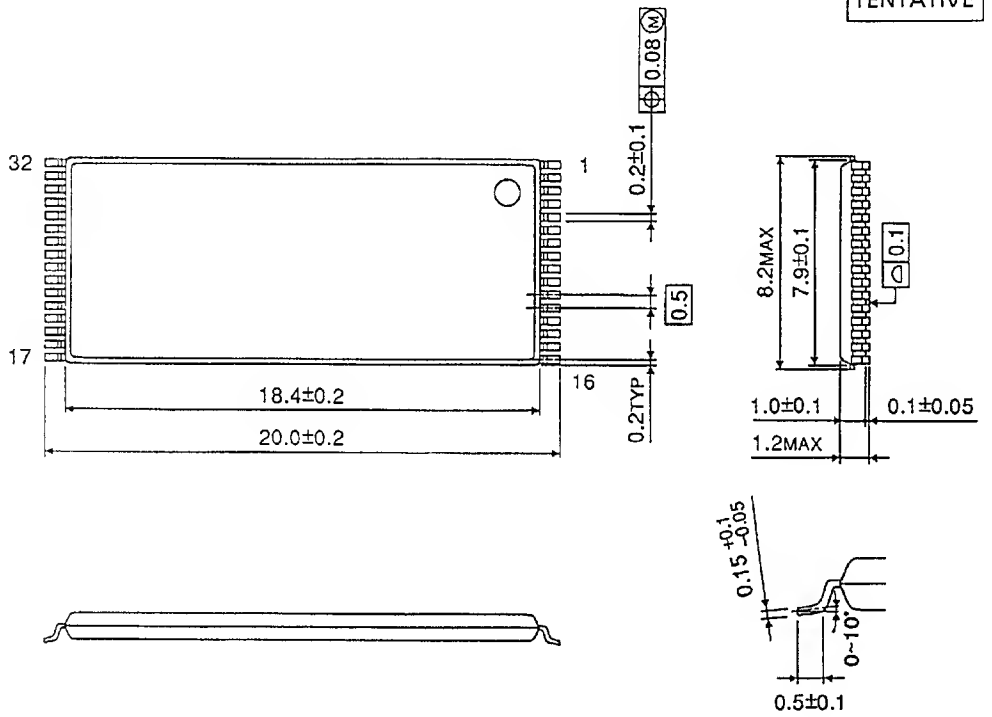
Weight : 0.36 g (Typ.)

TC518129AFTL-80LV
TC518129AFTL-10LV
TC518129AFTL-12LV

OUTLINE DRAWING (TSOP32 - P - 0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

TC518129ATRL-80LV
TC518129ATRL-10LV
TC518129ATRL-12LV

524,288 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

PRELIMINARY

DESCRIPTION

The TC518512PL Family is a 4M bit high speed CMOS Pseudo Static RAM organized as 524,288 words by 8 bits. The TC518512PL Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{OE}$/$\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518512PL Family has a static RAM-like write functionality where input data is written into the memory cell at the rising edge of R/W, which allows easy interfacing with microprocessor.

The TC518512PL Family is packaged in a 32 pin standard 0.6 inch width plastic DIP, Small Out line plastic flat Package and Thin Small Outline Package.

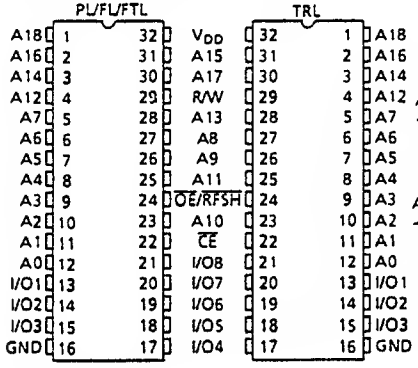
FEATURES

- Organization: 4M bit (524,288 word × 8bit)
- Fast Access Time and Low Power Dissipation

	TC518512PL Family		
	-70	-80	-10
t_{CEA} $\overline{CE}$ Access Time	70ns	80ns	100ns
t_{OEA} $\overline{OE}$ Access Time	30ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	200μA		

- Single Power Supply : 5V±10%
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 2048 refresh cycle / 32ms
- Logic Compatible: SRAM R/W Pin
- Package : TC518512PL : DIP32-P-600
  : TC518512FL : SOP32-P-525
  : TC518512FTL : TSOP32-P-400
  : TC518512TRL : TSOP32-P-400A

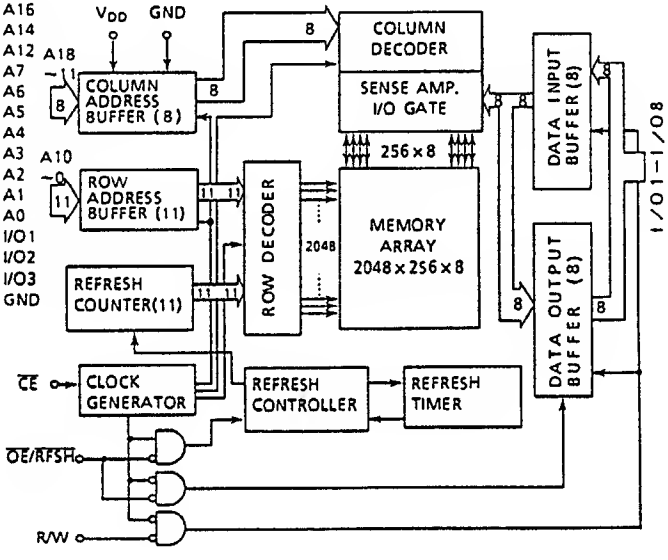
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A18	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$/$\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	$\overline{OE}$/RFSH	R/W	A0 ~ A18	I/O1 ~ 8	CONDITION
L	L	H	V*	OUT	Read
L	*	L	V*	IN	Write
L	H	H	V*	HZ	$\overline{CE}$ only Refresh
H	L	*	*	HZ	Auto/Self Refresh
H	H	*	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLOER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_O	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{OO}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
I_{DDD}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: $t_{RC} = t_{RC}$ min.	70ns version	-	50	70	mA	3, 4
		80ns version	-	45	60		
		100ns version	-	35	50		
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IH}$		-	-	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE/RFSH} = V_{DD} - 0.2V$		-	-	200	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IL}$		-	-	1	mA	
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE} = V_{DD} - 0.2V$, $\overline{OE/RFSH} = 0.2V$		-	100	200	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{OE/RFSH}$ cycling : tFC = tFC min)		-	-	2	mA	
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average Current) ($\overline{CE}$, Address cycling : tRC = tRC min)	70ns version	-	-	70	mA	3
		80ns version	-	-	60		
		100ns version	-	-	50		
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V		-10	-	10	μA	
$I_{D(L)}$	Output Leakage Current Output Disable ($\overline{CE} = V_{IH}$ or $\overline{OE/RFSH} = V_{IH}$ or R/W = V_{IL}), $0V \leq V_{DUT} \leq V_{DD}$		-10	-	10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0mA$		2.4	-	-	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$		-	-	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A18)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE/RFSH}$, R/W)	-	7	pF
C_{IO}	Input/Output Capacitance	-	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

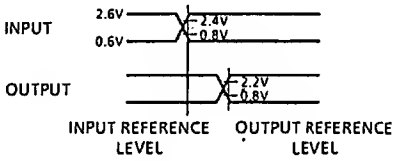
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	-	130	-	160	-	ns	
t_{RMW}	Read Modify Write Cycle Time	165	-	180	-	220	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	35	-	40	-	50	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	70	-	80	-	100	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	30	-	30	-	40	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	20	-	20	-	20	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25	ns	9
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	9
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	25	-	25	-	30	-	ns	
t_{WCH}	Write Command Hold Time	40	-	40	-	50	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	-	25	-	30	-	ns	
t_{OSW}	Data Set-Up Time from R/W	20	-	20	-	25	-	ns	10
t_{OSC}	Data Set-Up Time from $\overline{CE}$	20	-	20	-	25	-	ns	10
t_{OHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{OHC}	Data Hold Time from $\overline{CE}$	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	15	-	20	-	25	-	ns	11
t_{FC}	Auto Refresh Cycle Time	130	-	130	-	160	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	-	40	-	50	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	$\overline{CE}$ Delay Time form $\overline{RFSH}$ (Self Refresh)	160	-	160	-	190	-	ns	12
t_{REF}	Refresh Period (2048 cycle, A0~A10)	-	32	-	32	-	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} and I_{DDF4} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements asuume t_T = 5ns.
7) Timing reference level

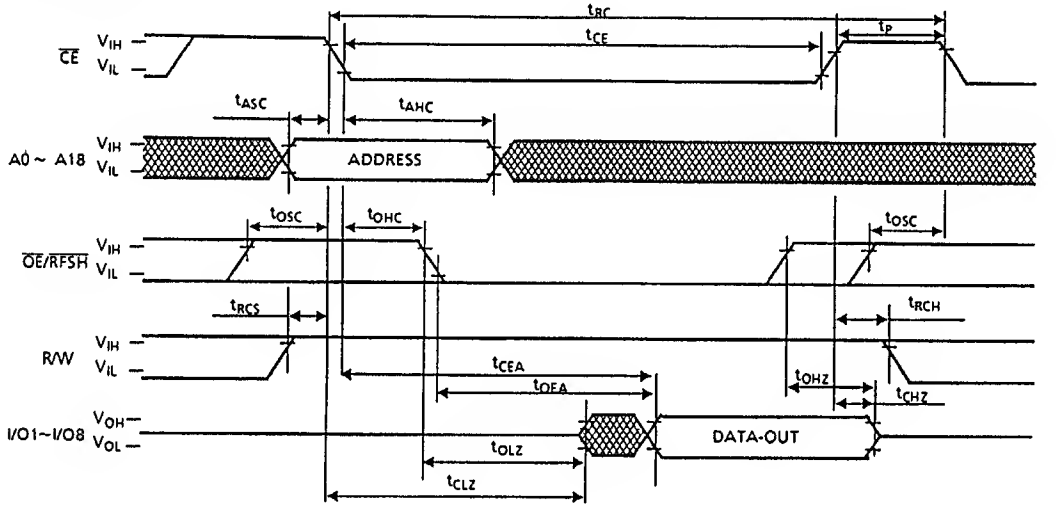
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level:		V_{OH} = 2.2V
		V_{OL} = 0.8V



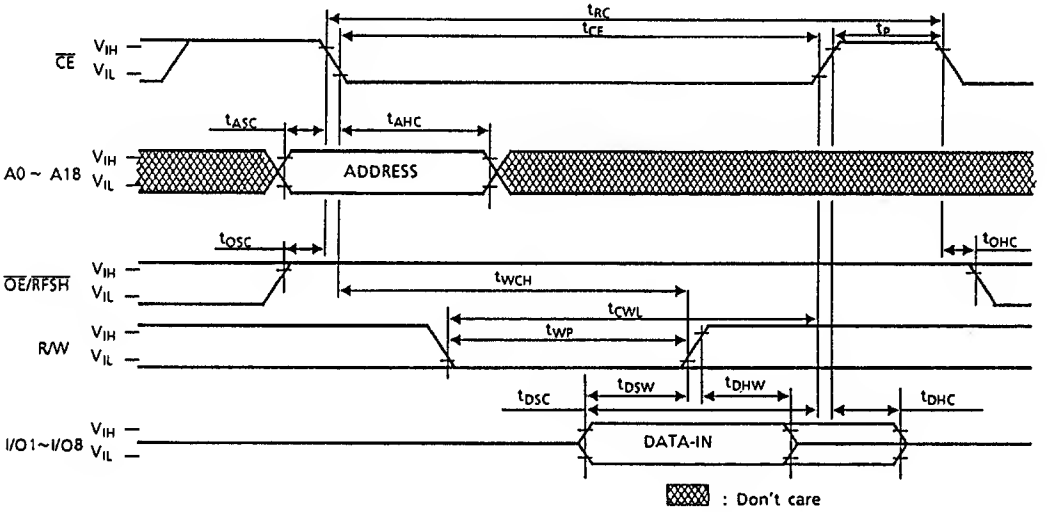
8) Measured with a load equivalent to 1 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DIIW} or t_{DIIC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{OE}/\overline{RFSH}$ = "L" after power-up

TIMING WAVEFORMS

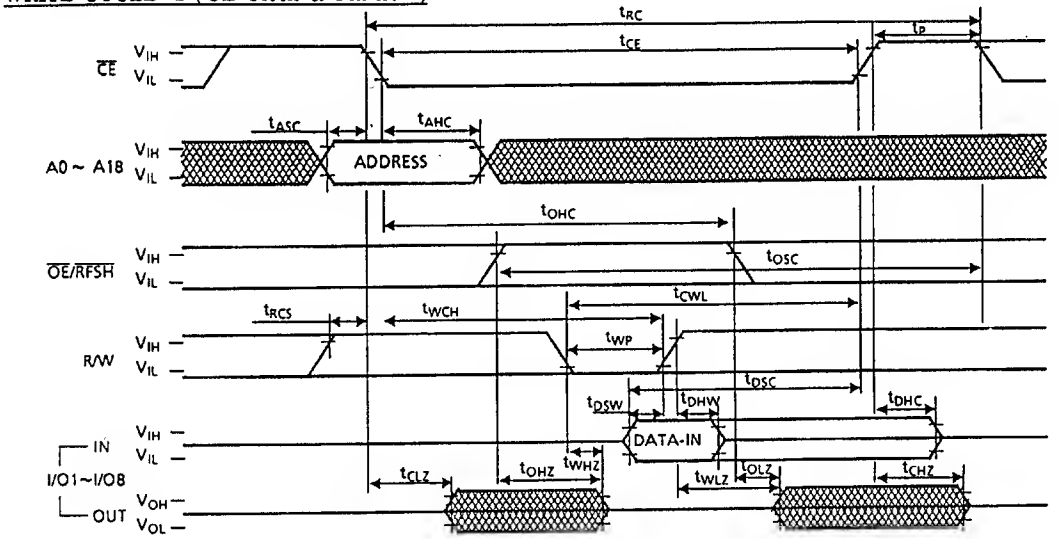
READ CYCLE



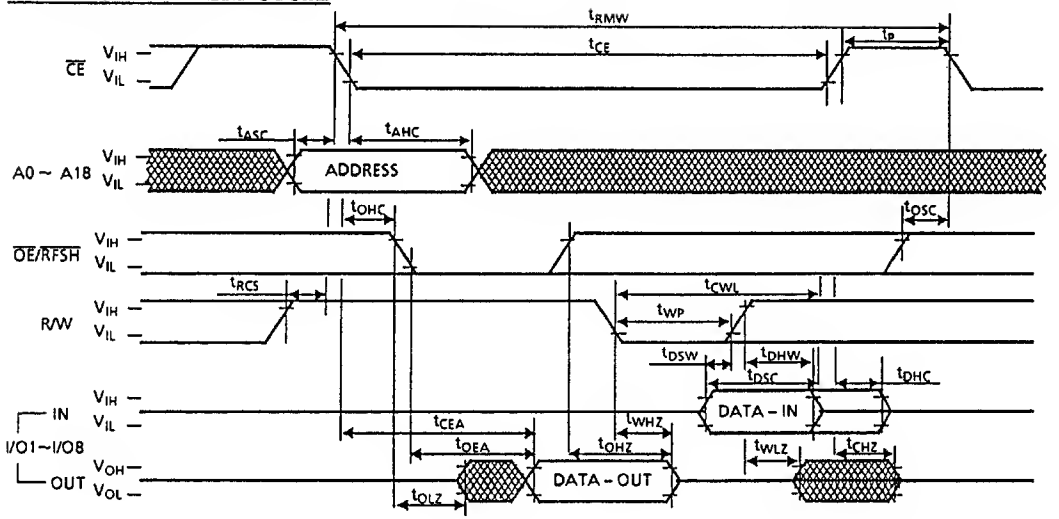
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



WRITE CYCLE - 2 ($\overline{OE}$ Clock & Fix Low)

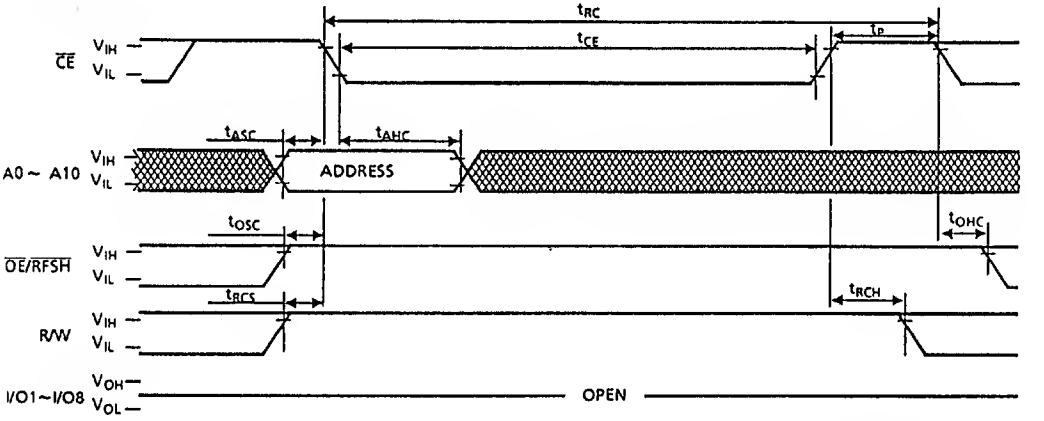


READ MODIFY WRITE CYCLE



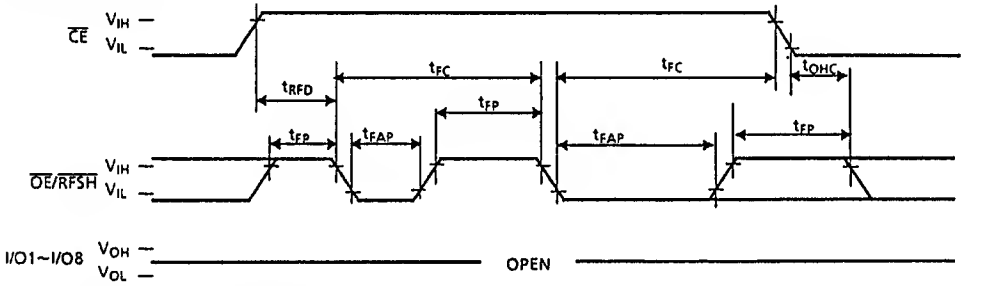
: Don't care

$\overline{CE}$ ONLY REFRESH



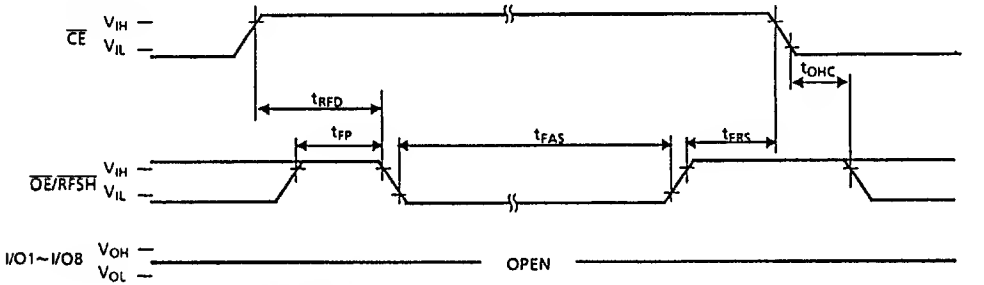
NOTE : A11 ~ A16 = Don't care, ▨ : Don't care

AUTO REFRESH



NOTE : R/W, A0 ~ A18 = Don't care

SELF REFRESH

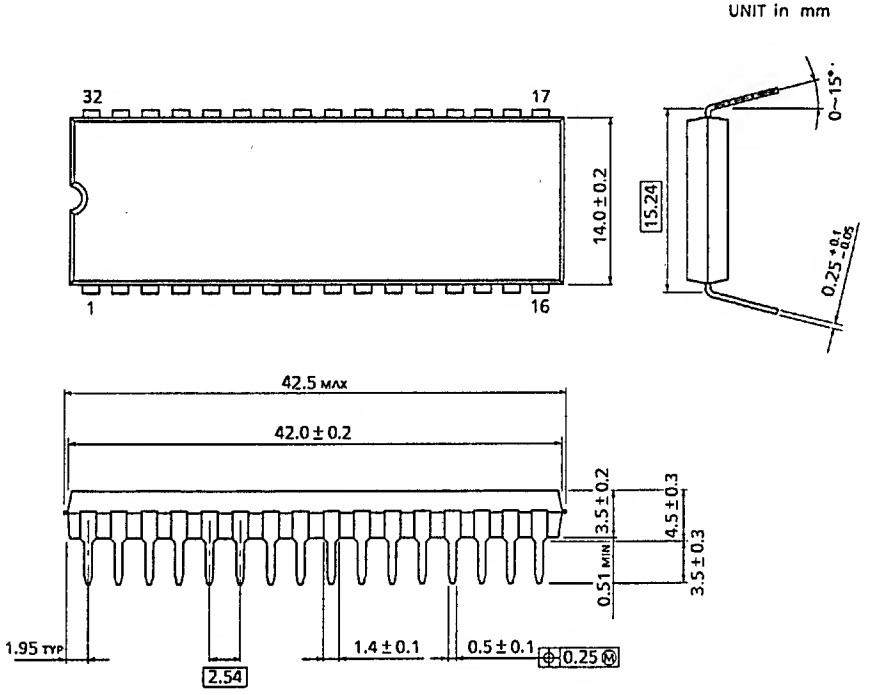


NOTE : R/W, A0 ~ A18 = Don't care

OUTLINE DRAWINGS

(DIP32-P-600)

UNIT in mm



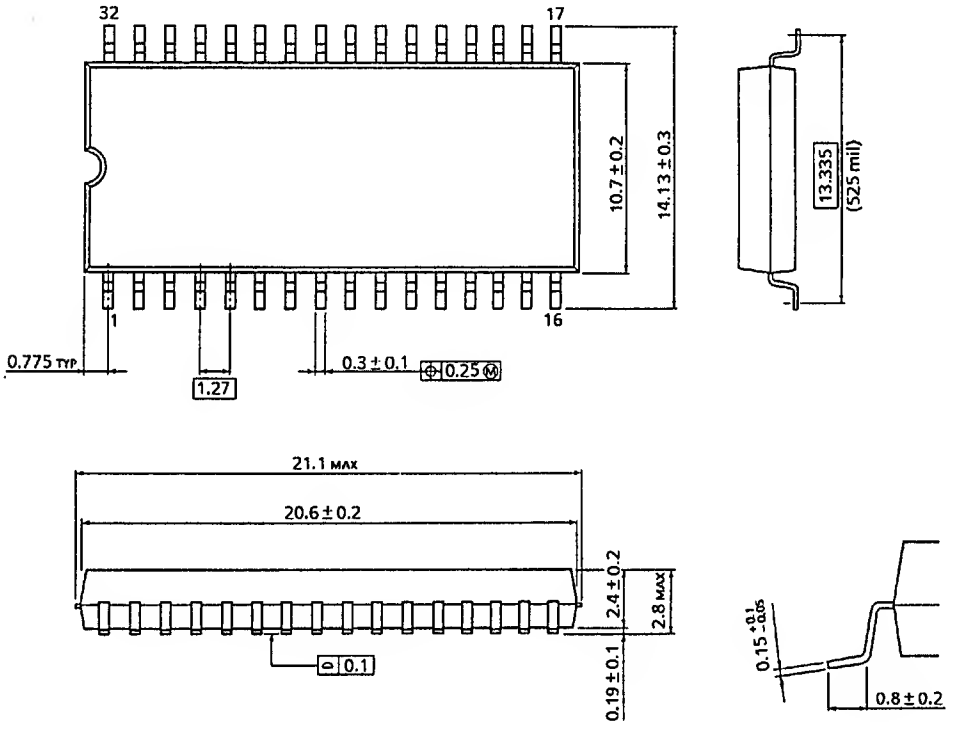
Weight : 4.53g (TYP.)

TC518512PL-70, -80, -10

OUTLINE DRAWINGS

(SOP32−P−525)

UNIT in mm



Weight : 1.10g (TYP.)

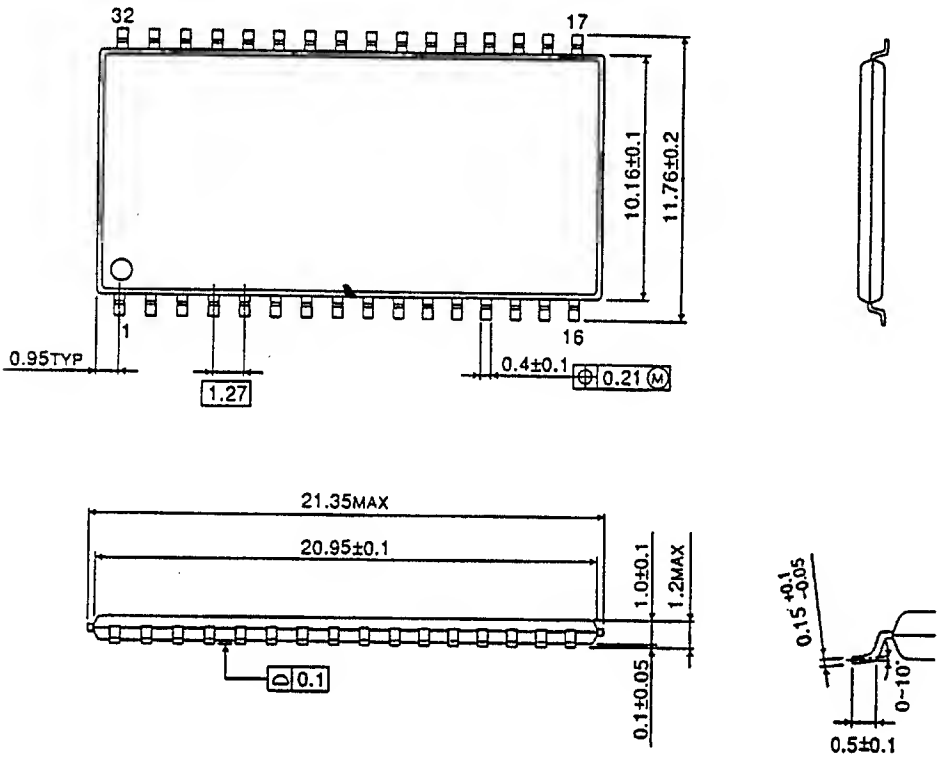
TC518512FL-70, -80, -10

OUTLINE DRAWINGS

(TSOP32−P−400)

TENTATIVE

UNIT in mm



Weight: 0.51g (Typ.)

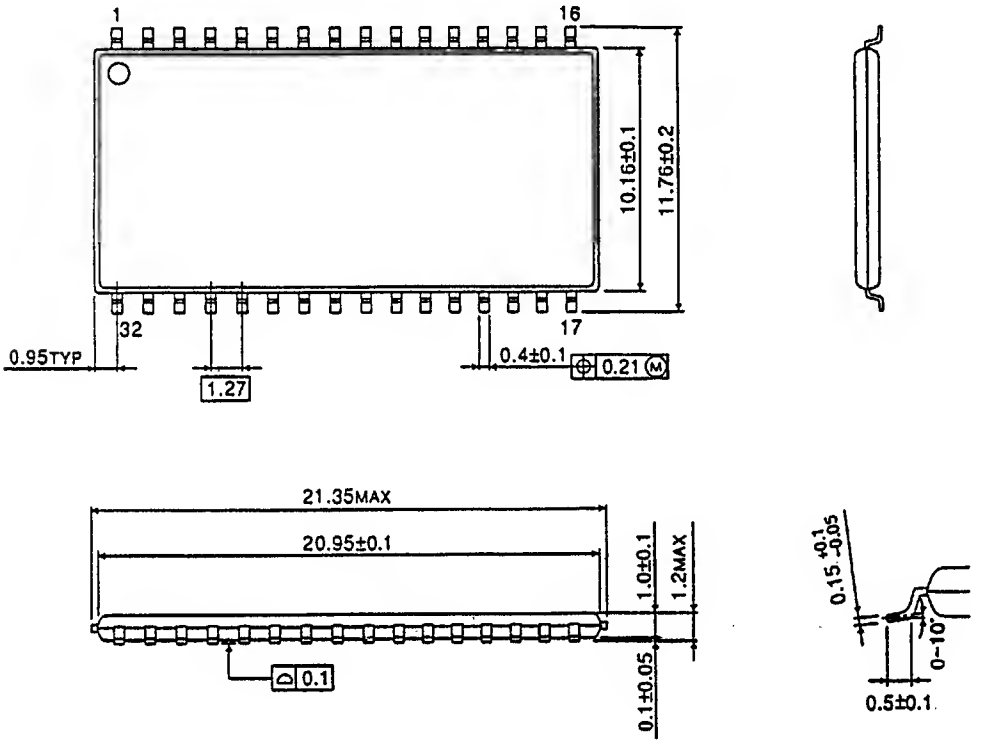
TC518512FTL-70, -80, -10

OUTLINE DRAWINGS

(TSOP32−P−400A)

TENTATIVE

UNIT in mm



Weight: 0.51g (Typ.)

TC518512TRL-70, -80, -10

CMOS Static RAM

32,768 WORDS × 8 BIT STATIC RAM **PRELIMINARY**

DESCRIPTION

The TC55257BPL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5 V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85 ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 100 μA. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in a standard dual-in-line 28 pin plastic package (0.6 / 0.3 inch width), small-out-line plastic package and thin-small-out-line plastic package (forward type, reverse type).

FEATURES

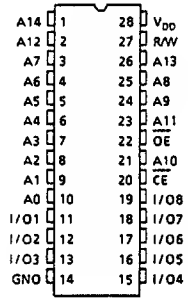
- Low Power Dissipation
  27.5 mW / MHz (Typ.) Operating
- Standby Current : 100 μA (MAX.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE}$
- Data retention Supply Voltage : 2.0~5.5 V
- Directly TTL Compatible
  : All Inputs and Outputs
- Access Time

	TC552578PL/BFL/ BSPL/BFTL/BTRL-85	TC552578PL/8FL/ BSPL/BFTL/BTRL-10
Access Time (max.)	85 ns	100 ns
Chip Enable Access Time (max.)	85 ns	100 ns
Output Enable Time (max.)	45 ns	50 ns

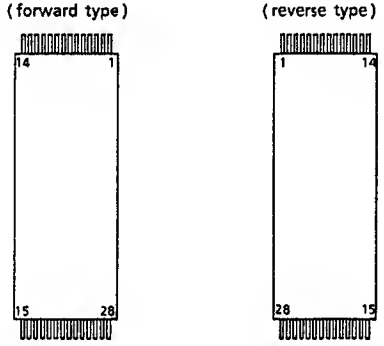
- Package
  TC55257BPL : DIP28-P-600
  TC55257BFL : SOP28-P-450
  TC55257BSPL : DIP28-P-300B
  TC55257BFTL : TSOP28-P
  TC55257BTRL : TSOP28-P-A

PIN CONNECTION (TOP VIEW)

o 28 PIN DIP & SOP



o 28 PIN TSOP

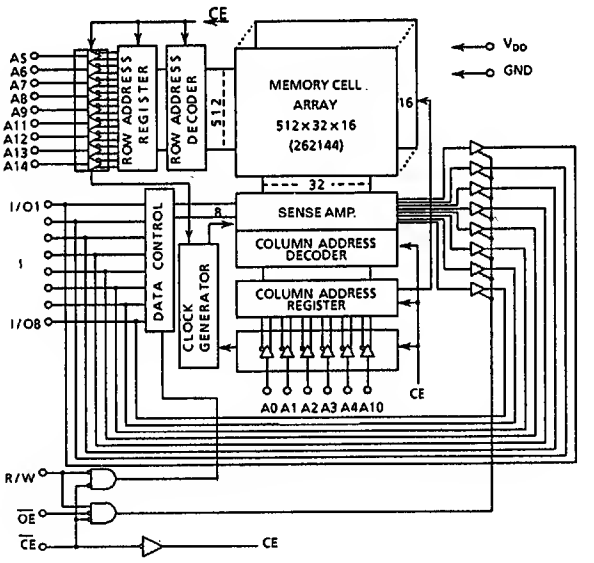


PIN NAME

A0~A14	Address Inputs
R / W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I / O1~I / O8	Data Input / Output
V_{DD}	Power (+ 5 V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

* : −3.0 V at pulse width 50 ns

** : 0.6 inch 1.0 W, 0.3 inch 0.8 W, 0.45 inch 0.6 W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	- 0.3*	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

* : -3.0 V at pulse width 50 ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70$ °C, $V_{DD} = 5\ V \pm 10\ \%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		-	-	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\ V$		- 1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\ V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		-	-	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH} / V_{IL} $I_{OUT} = 0$ mA	$t_{cycle} = 1\ \mu s$	-	10	-	mA
			t_{cycle} = Min. cycle	-	-	70	
I_{DDO2}		$\overline{CE} = 0.2\ V$ $R/W = V_{DD} - 0.2\ V$ Other Input $= V_{DD} - 0.2\ V / 0.2\ V$ $I_{OUT} = 0$ mA	$t_{cycle} = 1\ \mu s$	-	5	-	mA
			t_{cycle} = Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2$, $V_{DD} = 2.0V \sim 5.5V$, $Ta = 0 \sim 70$ °C		-	2	100	μA

CAPACITANCE ($Ta = 25$ °C, $f = 1$ MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	

Note : This parameter periodically sampled is not 100 % tested.

A.C. CHARACTERISTICS (Ta = 0~70 °C, V_{DD} = 5 V ± 10 %)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/B5PL/BFTL/BTRL-B5		TC55257BPL/BFL/B5PL/BFTL/BTRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	B5	–	100	–	ns
t_{ACC}	Address Access Time	–	B5	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	B5	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/B5PL/BFTL/BTRL-B5		TC55257BPL/BFL/B5PL/BFTL/BTRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	B5	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	
t_{ODW}	R/W to Output in High-Z	–	30	–	50	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Set up Time	40	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

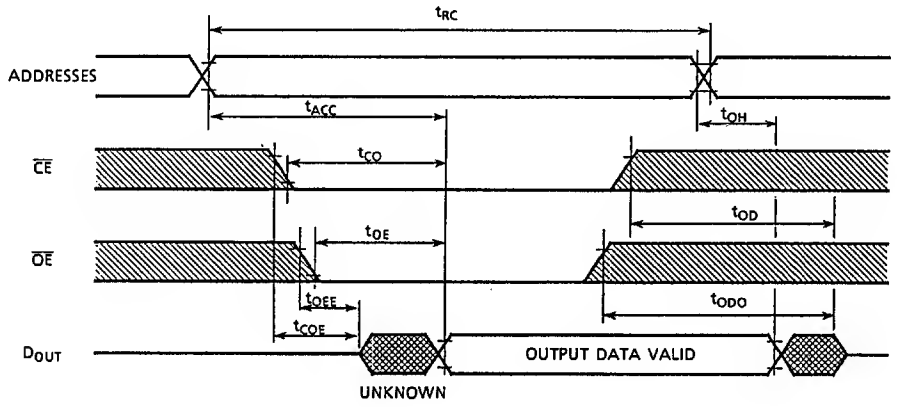
A.C. Test Conditions

Output Load	:	100 pF + 1 TTL Gate
Input Pulse Level	:	0.6 V, 2.4 V
Timing Measurement	:	0.8 V, 2.2 V
Reference Level	:	0.8 V, 2.2 V
t_r, t_f	:	5 ns

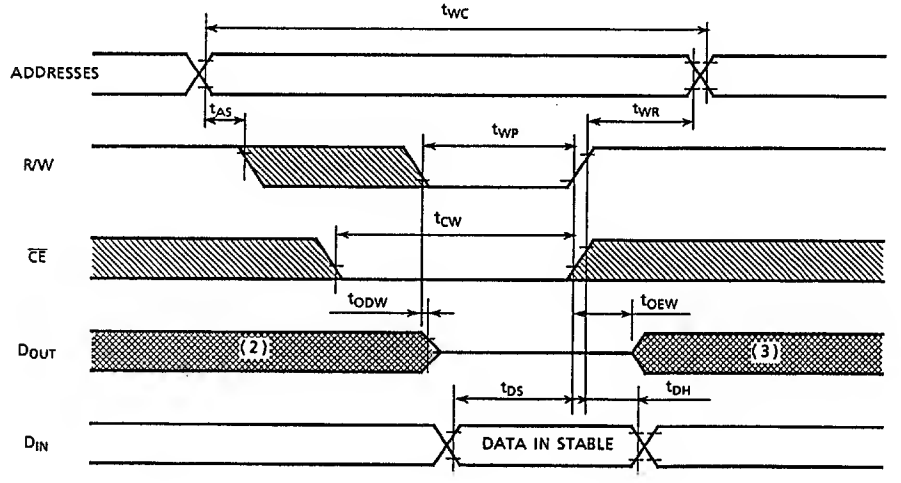
•

TIMING WAVEFORMS

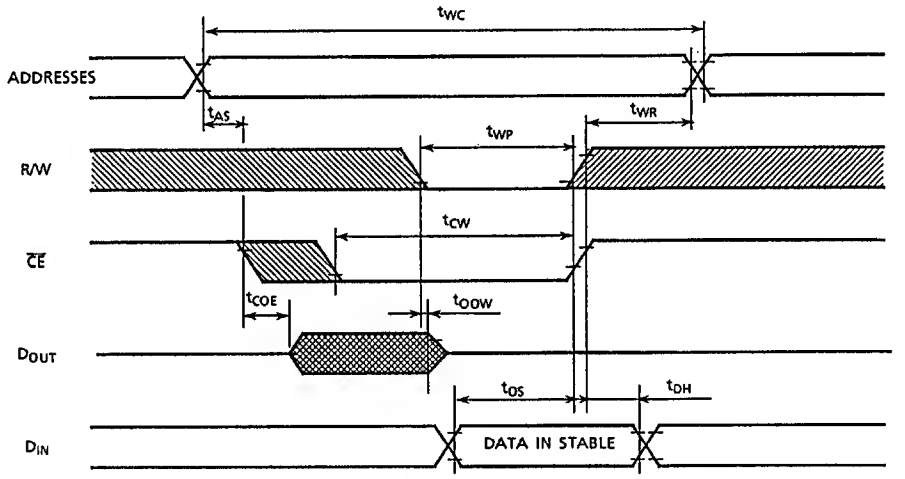
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Note : (1) R/W is High for read cycle.

(2) Assuming that $\overline{CE}$ low transition occurs coincident with or after R / W Low transition, Outputs remain a high impedance state.

(3) Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R / W High transition, Outputs remain a high impedance state.

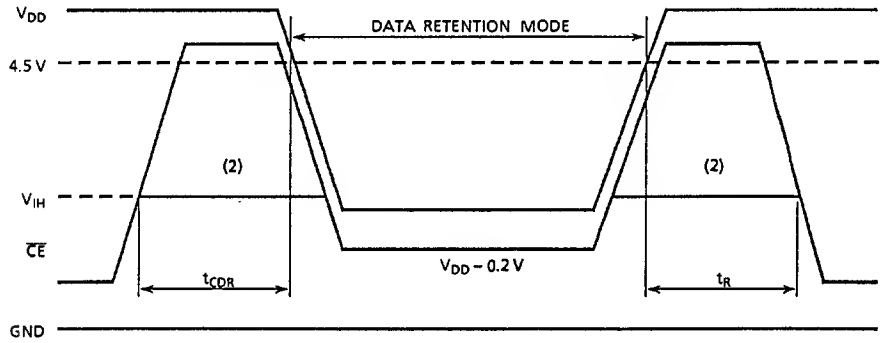
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0~70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0 V	-	-	50	μA
		V_{DH} = 5.5 V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC} (1)	-	-	

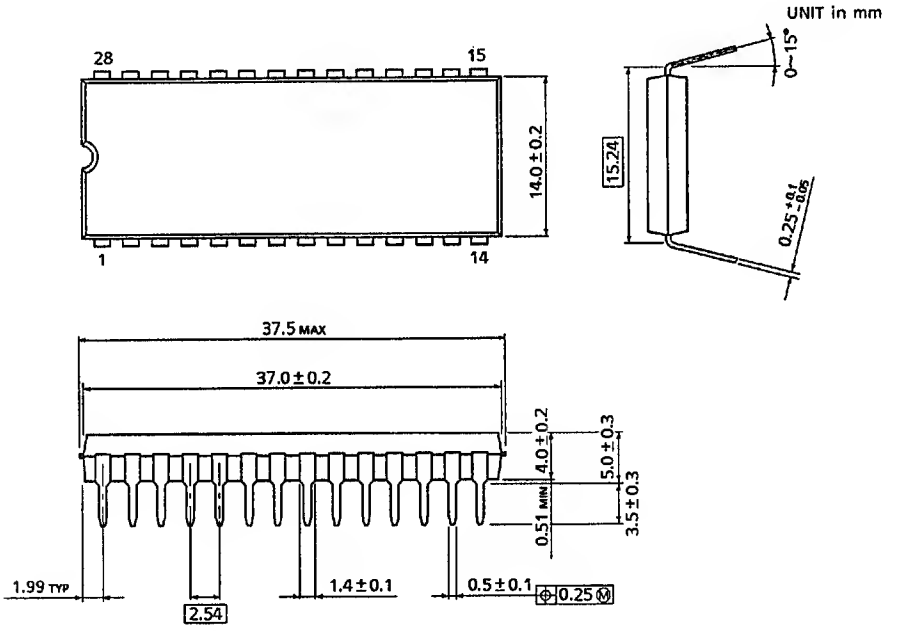
Note (1) : Read Cycle Time.

$\overline{CE}$ Controlled Data Retention Mode



Note (2) : If the V_{IH} of $\overline{CE}$ is 2.2 V in opertion, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5 V to 2.4 V

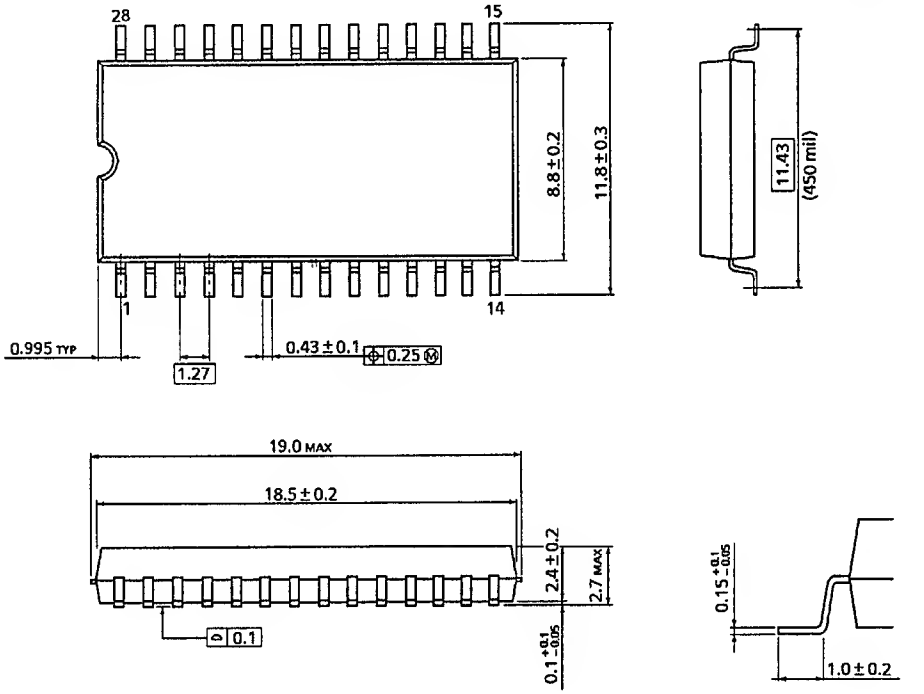
OUTLINE DRAWINGS (DIP28 – P – 600)



Weight : 4.43g (Typ.)

OUTLINE DRAWINGS (SOP28 – P – 450)

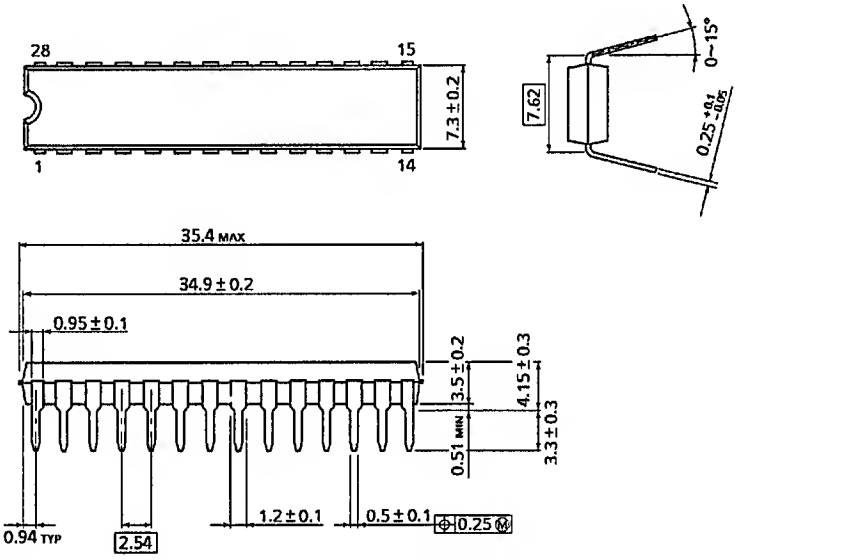
Unit in mm



Weight : 0.79g (Typ.)

OUTLINE DRAWINGS (DIP28 – P – 300B)

UNIT in mm

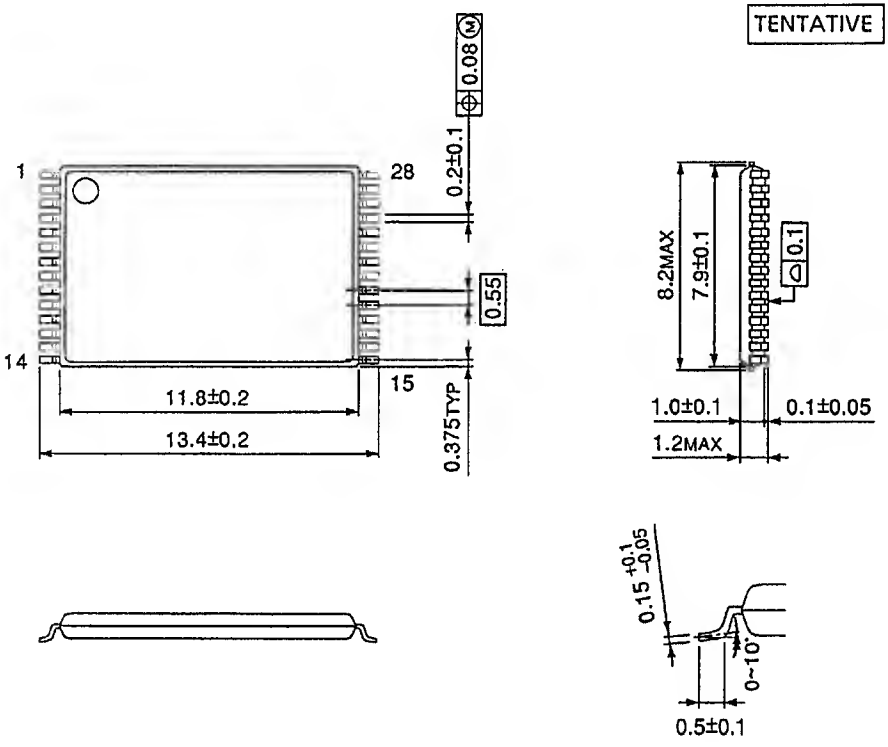


Weight : 2.04g (Typ.)

OUTLINE DRAWINGS (TSOP28 - P)

UNIT in mm

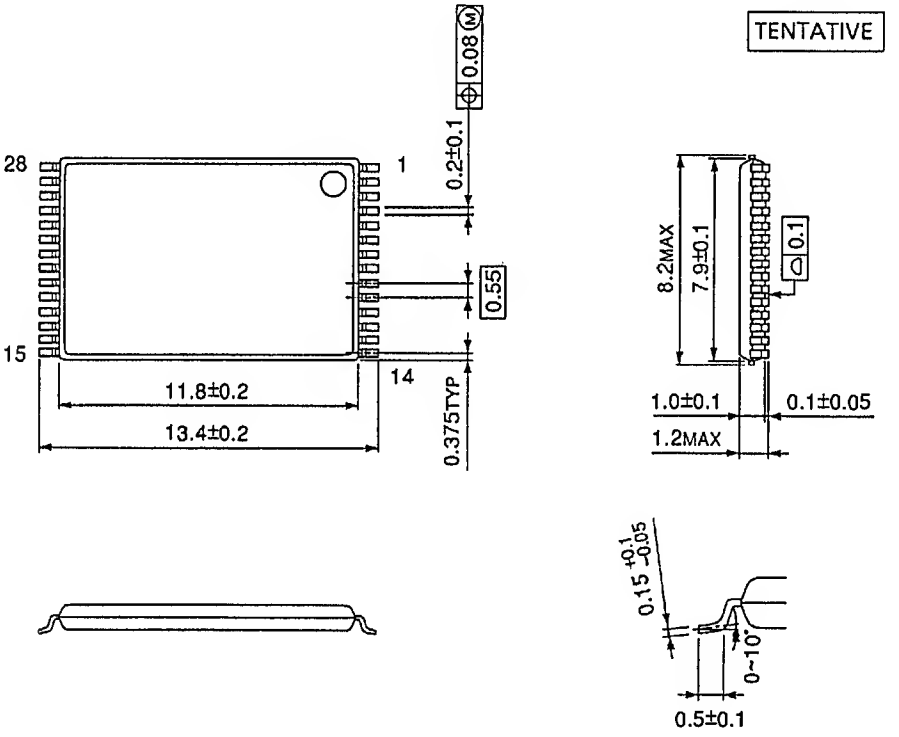
TENTATIVE



OUTLINE DRAWINGS (TSOP28 – P – A)

UNIT in mm

TENTATIVE



32,768 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55257BPL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5 V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85 ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2 μA at room temperature. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in a standard dual-in-line 28 pin plastic package (0.6 / 0.3 inch width), small-out-line plastic package and thin-small-out-line plastic package (forward type, reverse type).

FEATURES

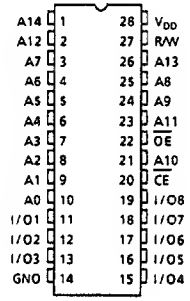
- Low Power Dissipation
  27.5 mW / MHz (Typ.) Operating
- Standby Current : 2μA (MAX.) at Ta = 25°C
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE}$
- Data retention Supply Voltage : 2.0~5.5 V
- Directly TTL Compatible
  : All Inputs and Outputs
- Access Time

	TC55257BPL/BFL/ B5PL/BFTL/BTRL-B5L	TC55257BPL/BFL/ B5PL/BFTL/BTRL-10L
Access Time (max.)	85 ns	100 ns
Chip Enable Access Time (max.)	85 ns	100 ns
Output Enable Time (max.)	45 ns	50 ns

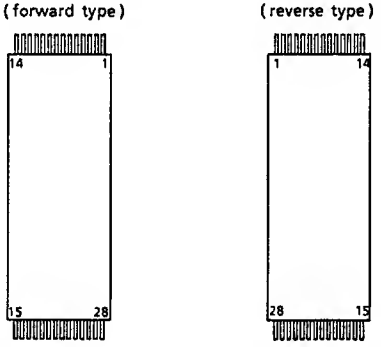
- Package
  TC55257BPL : DIP28-P-600
  TC55257BFL : SOP28-P-450
  TC55257BSPL : DIP28-P-300B
  TC55257BFTL : TSOP28-P
  TC55257BTRL : TSOP28-P-A

PIN CONNECTION (TOP VIEW)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP

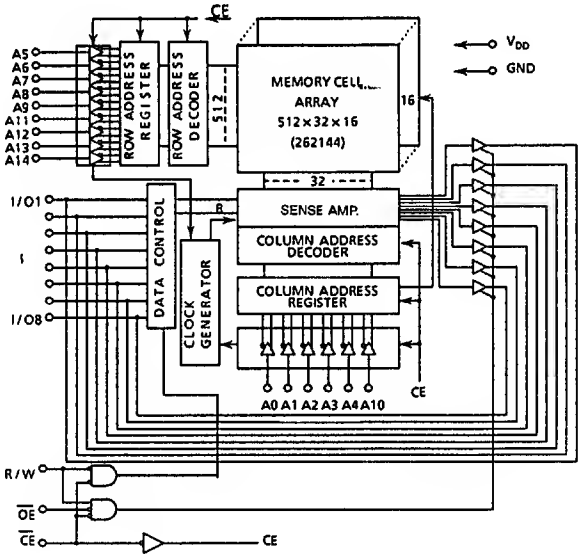


PIN NAME

A0~A14	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+5 V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

* : −3.0 V at pulse width 50 ns
** : 0.6 inch 1.0 W, 0.3 inch 0.8 W, 0.45 inch 0.6 W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	MIN.	MIN.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	– 0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* : –3.0 V at pulse width 50 ns

D.C. and OPERATING CHARACTERISTICS (T_a = 0~70 °C, V_{DD} = 5 V ± 10 %)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V		– 1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V		4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH} / V_{IL} I_{OUT} = 0 mA	t_{cycle} = 1 μs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2 V R/W = V_{DD} – 0.2 V Other Input = V_{DD} – 0.2 V / 0.2 V I_{OUT} = 0 mA	t_{cycle} = 1 μs	–	5	–	mA
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} – 0.2	T_a = 0~70 °C	–	–	30	μA
		V_{DD} = 2.0 V~5.5 V	T_a = 25 °C	–	–	2	μA

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note : This parameter periodically sampled is not 100 % tested.

A.C. CHARACTERISTICS (Ta = 0~70 °C, V_{DD} = 5 V ± 10 %)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/B5PL/BFTL/BTRL-85L		TC55257BPL/BFL/B5PL/BFTL/BTRL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

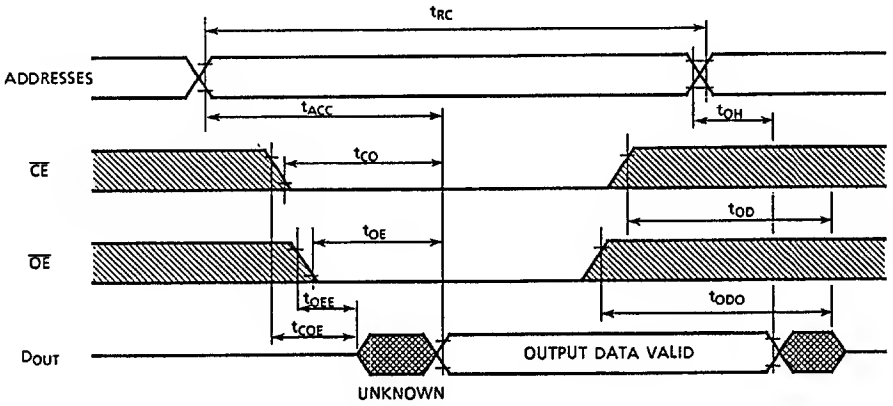
SYMBOL	PARAMETER	TC55257BPL/BFL/B5PL/BFTL/BTRL-85L		TC55257BPL/BFL/B5PL/BFTL/BTRL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	
t_{ODW}	R/W to Output in High-Z	–	30	–	50	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Set up Time	40	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

A.C. Test Conditions

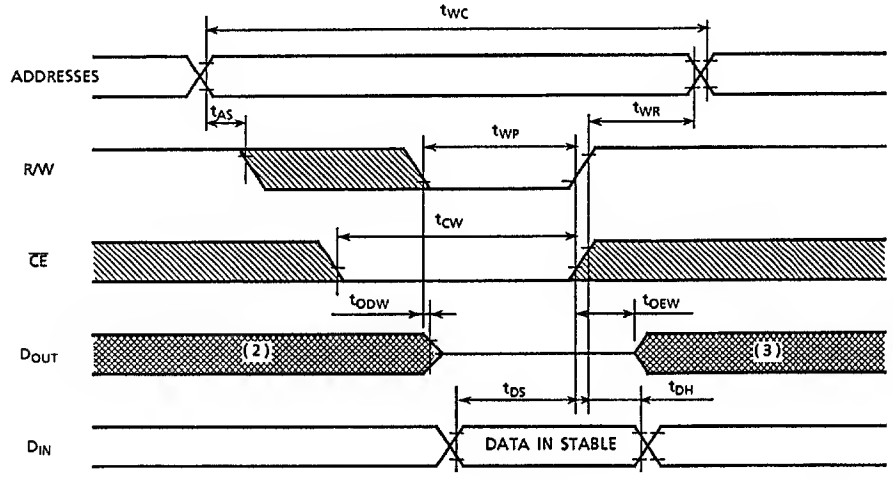
Output Load	:	100 pF + 1 TTL Gate
Input Pulse Level	:	0.6 V, 2.4 V
Timing Measurement	:	0.8 V, 2.2 V
Reference Level	:	0.8 V, 2.2 V
t_r, t_f	:	5 ns

TIMING WAVEFORMS

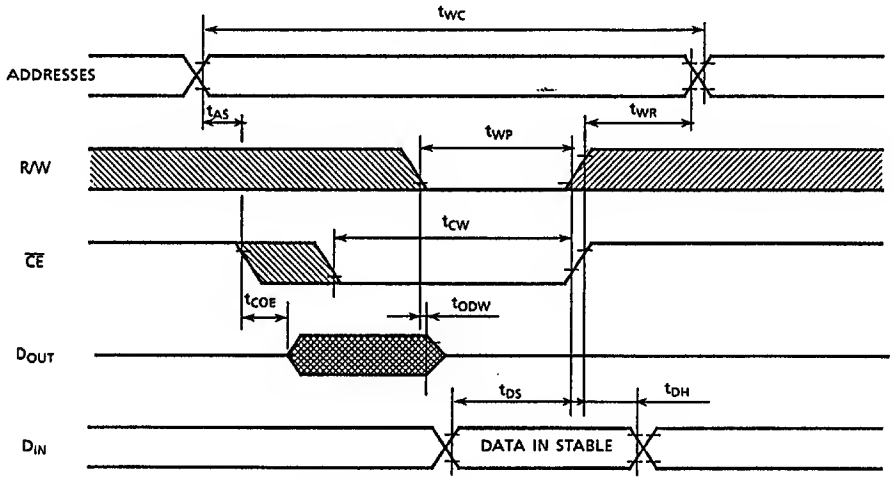
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Note : (1) R/W is High for read cycle.

(2) Assuming that $\overline{CE}$ low transition occurs coincident with or after R / W Low transition, Outputs remain a high impedance state.

(3) Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R / W High transition, Outputs remain a high impedance state.

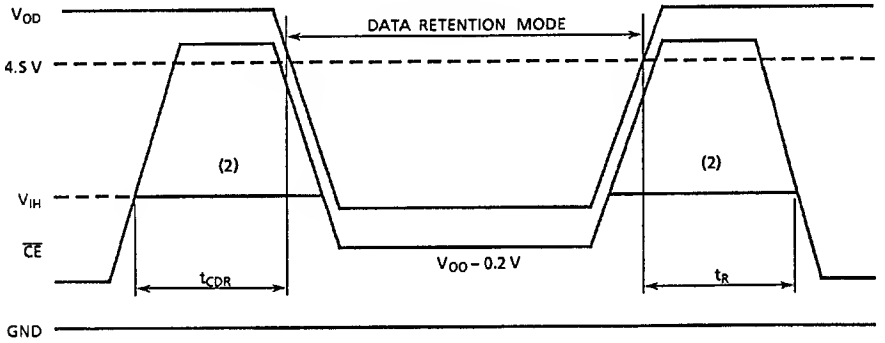
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0~70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{OH} = 3.0 V	-	-	20	μA
		V_{OH} = 5.5 V	-	-	30	
t_{COR}	Chip Deselection to Data Retention Mode		0	-	-	μS
t_R	Recovery Time		t_{RC} (1)	-	-	

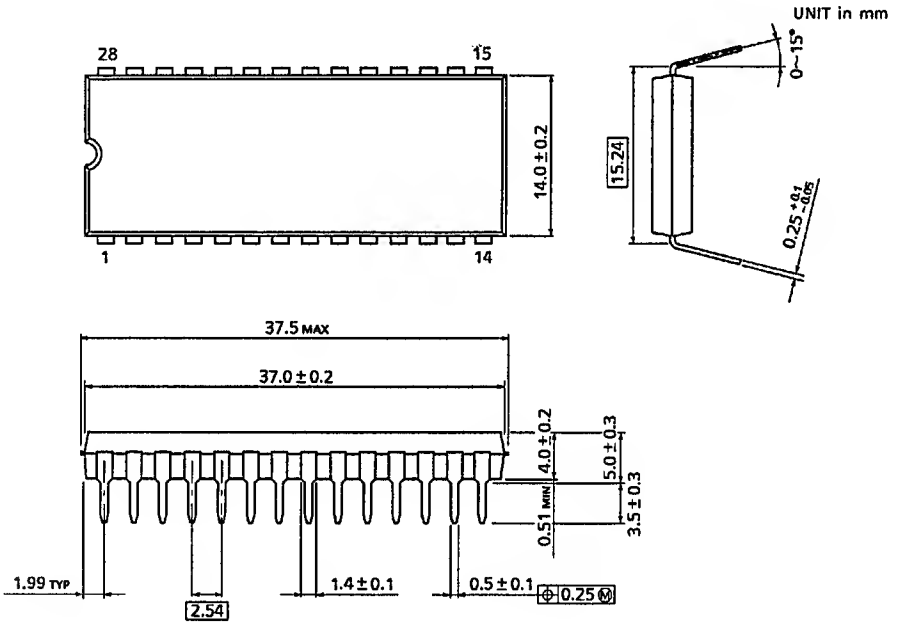
Note (1) : Read Cycle Time.

$\overline{CE}$ Controlled Data Retention Mode



Note (2) : If the V_{IH} of $\overline{CE}$ is 2.2 V in opertion, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5 V to 2.4 V

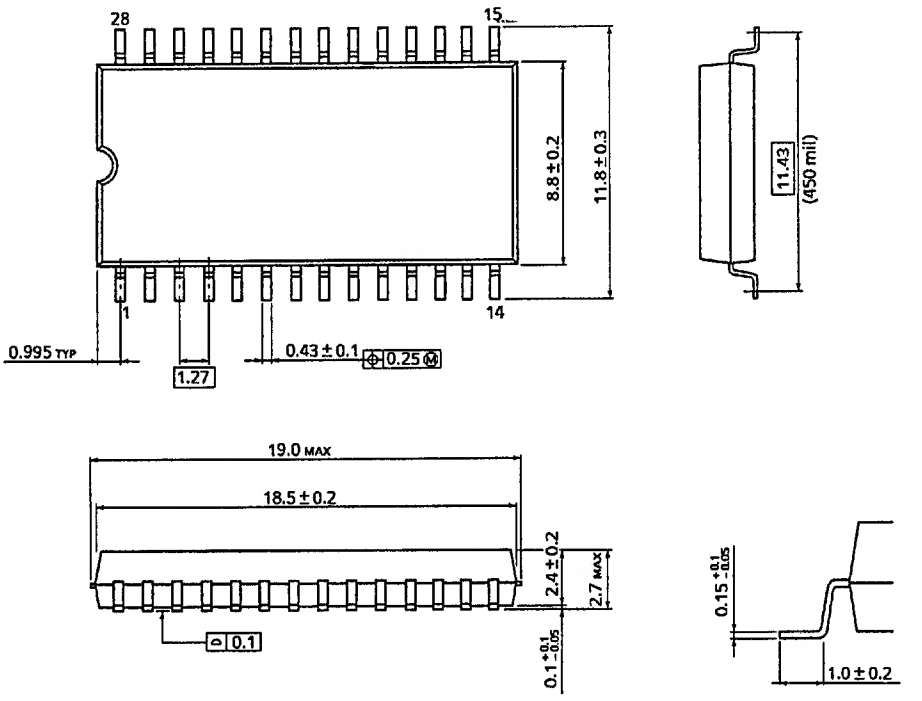
OUTLINE DRAWINGS (DIP28 - P - 600)



Weight : 4.43g (TYP.)

OUTLINE DRAWINGS (SOP28 – P – 450)

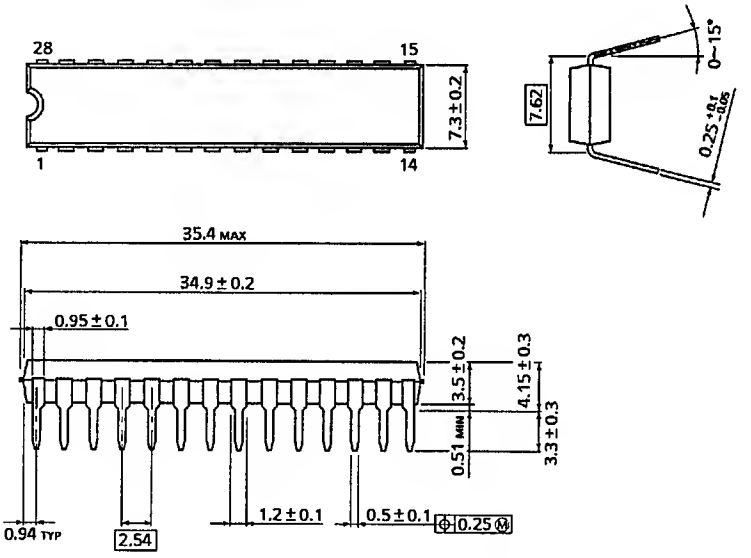
Unit in mm



Weight : 0.79g (TYP.)

OUTLINE DRAWINGS (DIP28 - P - 300B)

UNIT in mm

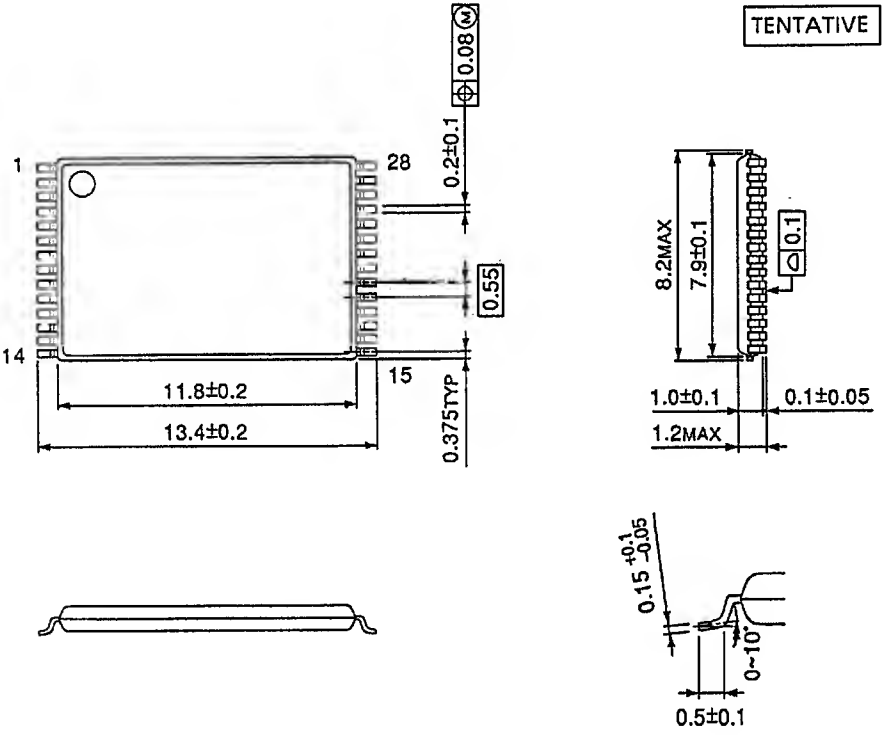


Weight : 2.04g (TYP.)

OUTLINE DRAWINGS (TSOP28 – P)

UNIT in mm

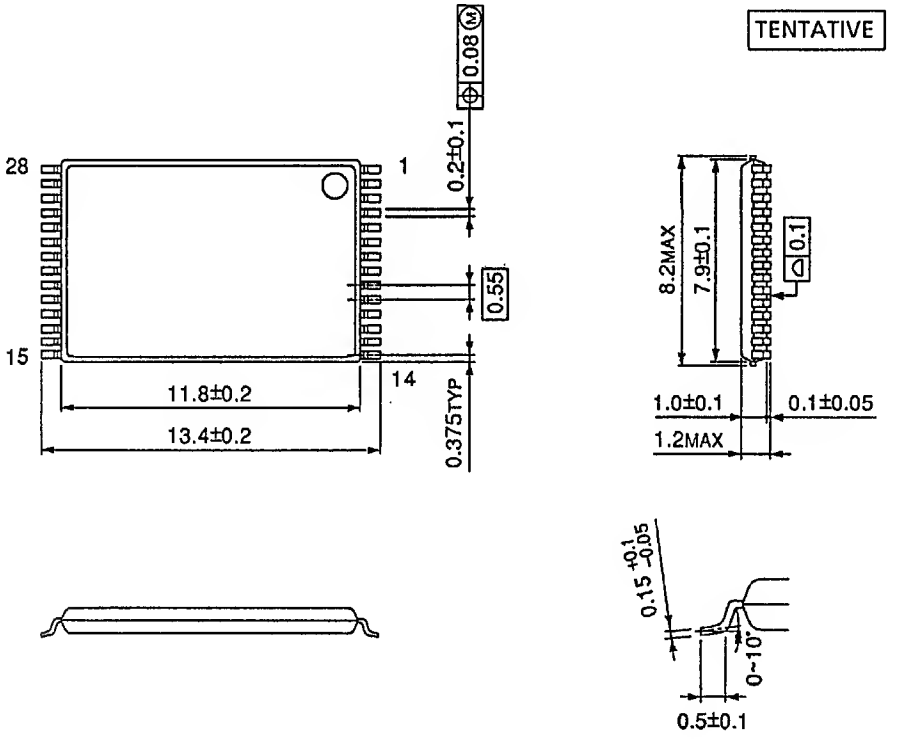
TENTATIVE



OUTLINE DRAWINGS (TSOP28 – P – A)

UNIT in mm

TENTATIVE



32,768 WORDS × 8 BIT STATIC RAM **PRELIMINARY**

DESCRIPTION

The TC55257BPI is 262,144 bit static ramdom access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA / MHz (Typ.) and maximum access time of 100ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA at room temperature.

The TC55257BPI has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPI is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. And TC55257BPI guarantees −40 ~ 85°C operating temperature so TC55257BPI is suitable for use in wide operating temperature system.

The TC55257BPI is offered in both a standard dual-in-line 28pin plastic package (0.6/0.3 inch width) and small-out-line plastic flat package.

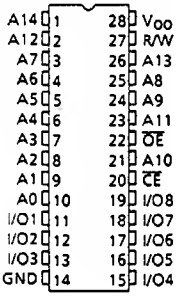
FEATURES

- Low Power Dissipation
  27.5mW / MHz (Typ.) Operating
- Standby Current
  2μA at Ta = 25°C (Max.) :
  TC55257BPI-10L / BFI-10L / BSPI-10L
- 5V Single Power Supply
- Power Down Feature : $\overline{CE}$
- Data retention Supply Voltage :
  2.0V ~ 5.5V
- Wide Temperature Operating :
  −40 ~ 85°C
- Access Time

	TC55257BPI-10L TC552578FI-10L TC55257B5PI-10L
Access Time (max.)	100ns
Chip Enable Access Time (max.)	100ns
Output Enable Time (Max.)	50ns

- Directly TTL Compatible: All Inputs and Outputs
- Package : TC55257BPI : DIP28−P−600
  TC55257BSPI : DIP28−P−300B
  TC55257BFI : SOP28−P−450

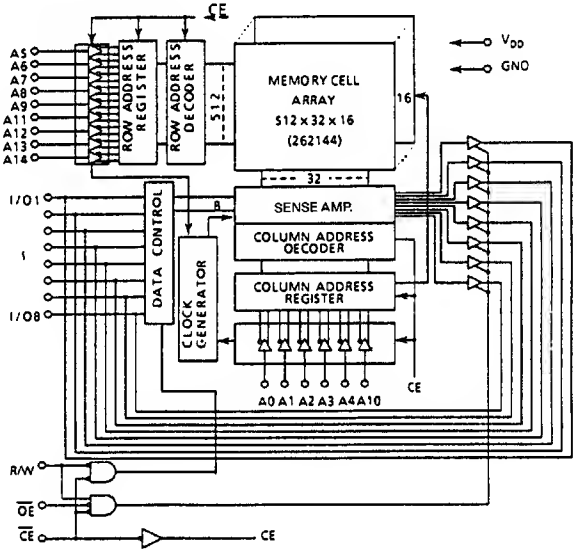
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg	Storage Temperature	-55~150	°C
Topr	Operating Temperature	-40~85	°C

*) -3.0V at pulse width 50ns
**) 0.6inch 1.0W, 0.3inch 0.8W, 0.45inch 0.6W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

*) -3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		−	−	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		−	−	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH} / V_{IL} I_{OUT} = 0mA	t_{cycle} = 1μs	−	10	−	mA
			t_{cycle} = Min. cycle	−	−	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V / 0.2V I_{OUT} = 0mA	t_{cycle} = 1μs	−	5	−	mA
			t_{cycle} = Min. cycle	−	−	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		−	−	3	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} − 0.2V V_{DD} = 2.0V~5.5V	Ta = −40~85°C	−	−	50	μA
			Ta = 25°C	−	−	2	

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55257BPI-10L TC55257BFI-10L TC55257BSPI-10L		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	100	–	ns
t_{ACC}	Address Access Time	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	100	
t_{OE}	Output Enable to Output in Valid	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	40	
t_{OH}	Output Data Hold Time	10	–	

WRITE CYCLE

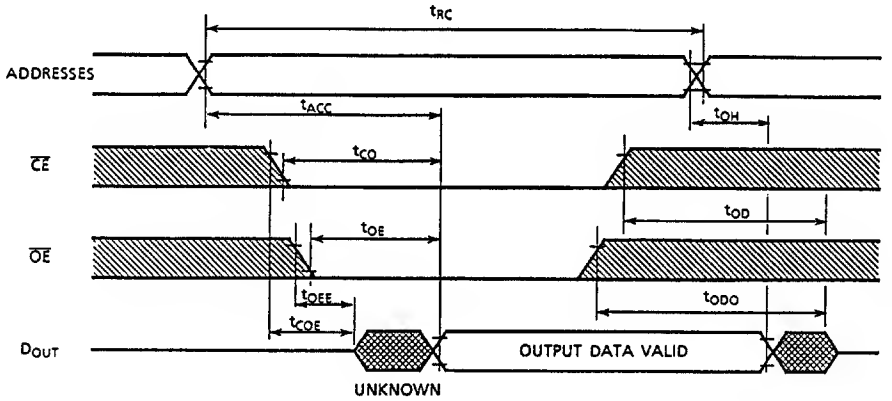
SYMBOL	PARAMETER	TC55257BPI-10L TC55257BFI-10L TC55257BSPI-10L		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	100	–	ns
t_{WP}	Write Pulse Width	70	–	
t_{CW}	Chip Selection to End of Write	90	–	
t_{AS}	Address Set up Time	0	–	
t_{WR}	Write Recovery Time	5	–	
t_{OOW}	R/W to Output High-Z	–	50	
t_{OEW}	R/W to Output Low-Z	0	–	
t_{DS}	Data Set up Time	40	–	
t_{DH}	Data Hold Time	0	–	

A.C. TEST CONDITIONS

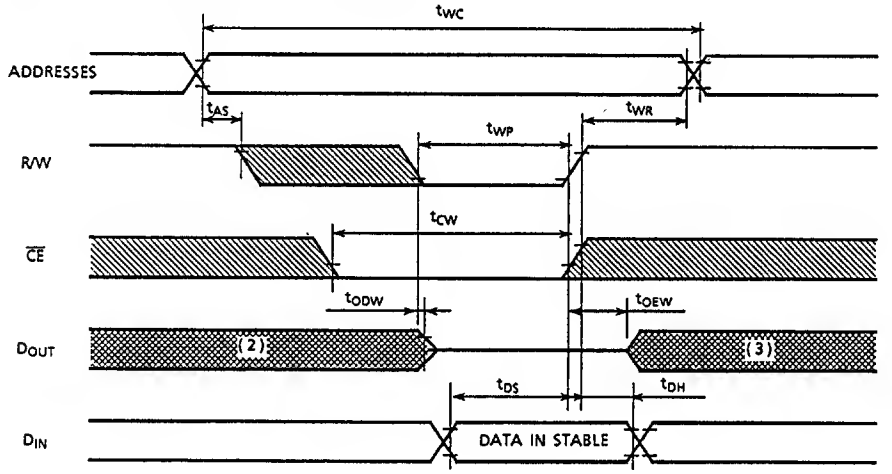
Output Load : 100pF + 1 TTL Gate
Input Pulse Level : 0.4V, 2.6V
Timing Measurement : 0.6V, 2.4V
Reference Level : 0.8V, 2.2V
t_r, t_f : 5ns

TIMING WAVEFROMS

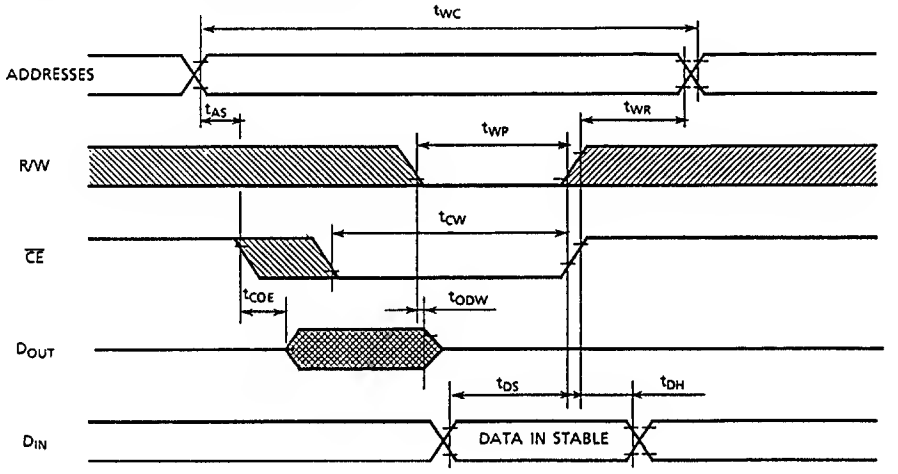
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for read cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain a high impedance state.

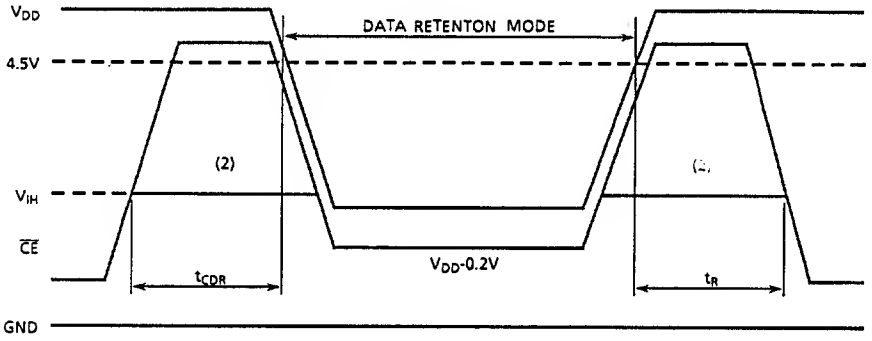
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = -40~85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	-	-	30	μA
		V_{DH} = 5.5V	-	-	50	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μS
t_R	Recovery Time		t_{RC} (1)	-	-	

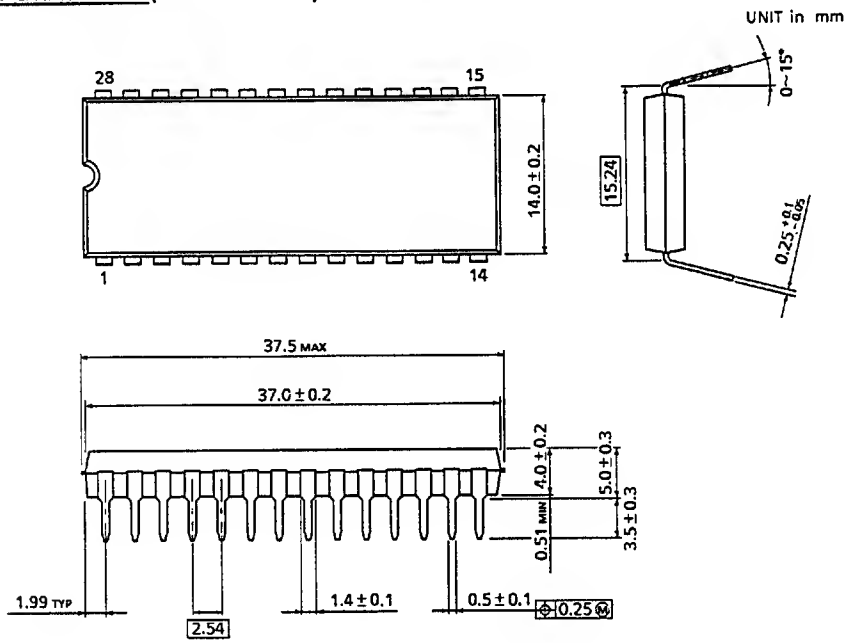
Note (1): Read Cycle Time.

CE Controlled Data Retention Mode



Note (2) : If the V_{IH} of $\overline{CE}$ is 2.4V in opertion, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V

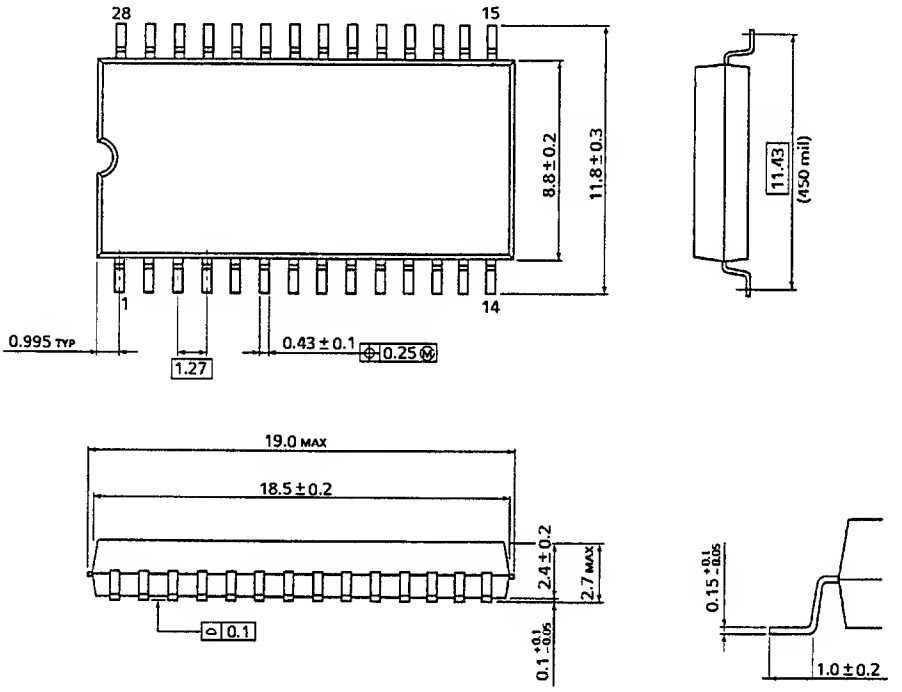
OUTLINE DRAWINGS (DIP28 - P - 600)



Weight : 4.43g (TYP.)

OUTLINE DRAWINGS (SOP28 - P - 450)

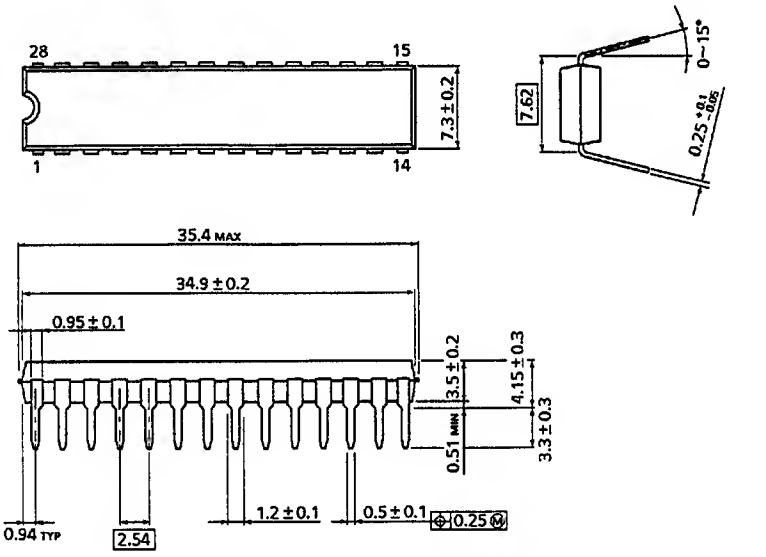
Unit in mm



Weight : 0.79g (TYP.)

OUTLINE DRAWINGS (DIP28-P-300B)

UNIT in mm



Weight : 2.04g (TYP.)

131,072 WORDS x 8 BIT STATIC RAM

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5 V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85/100 ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2 μA typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out line plastic flat package.

FEATURES

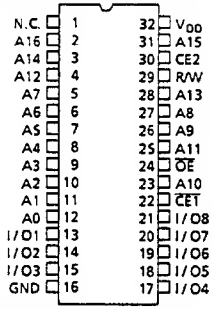
- Low Power Dissipation
  : 27.5 mW/MHz (Typ.)
- Standby Current : 100 μA (Max.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE1}$, CE2
- Data retention Supply Voltage : 2.0 ~ 5.5 V
- Directly TTL Compatible
  : All Inputs and Outputs

- Access Time

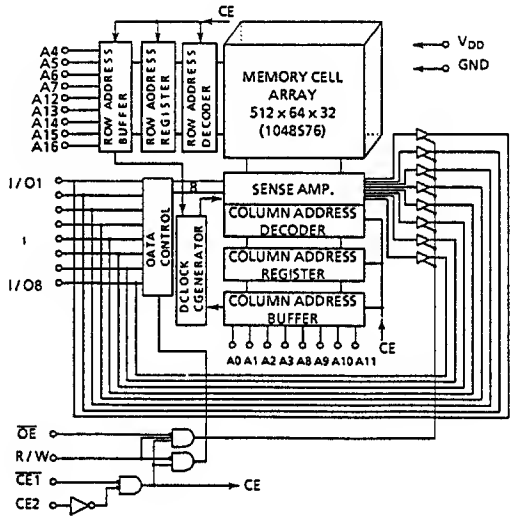
	TC551001 PL/FL-85	TC551001 PL/FL-10
Access Time (max.)	85 ns	100 ns
$\overline{CE1}$ Access Time (max.)	85 ns	100 ns
CE2 Access Time (max.)	85 ns	100 ns
$\overline{OE}$ Access Time (max.)	45 ns	50 ns

- Package : TC551001PL : DIP32-P-600
  TC551001FL : SOP32-P-525

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5 V)
GND	Ground
N.C.	No Connection

OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{OOS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{OO}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_O	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

* : −3.0 V at pulse width 50 ns MAX. ** : SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OO}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DO} + 0.3	
V_{IL}	Input Low Voltage	−0.3	−	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70\,°C$, $V_{DD} = 5\,V \pm 10\,\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\,V$	-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\,V$	4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/\overline{W} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/\overline{W} = V_{IH}$, $I_{OUT} = 0\,mA$, Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min. cycle	-	-	80	mA
I_{DDO2}		$\overline{CE1} = 0.2\,V$ and $CE2 = V_{DD}-0.2\,V$, $R/\overline{W} = V_{DD}-0.2\,V$, $I_{OUT} = 0\,mA$, Other Inputs = $V_{DD}-0.2\,V/0.2\,V$, t_{cycle} = Min. cycle	-	-	70	mA
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	-	-	3	mA
I_{DDS2} (1)		$\overline{CE1} = V_{DD}-0.2\,V$ or $CE2 = 0.2\,V$, $V_{DD} = 2.0\,V \sim 5.5\,V$, $Ta = 0 \sim 70\,°C$	-	2	100	μA

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2\,V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD}-0.2\,V$ or $CE2 \leqq 0.2\,V$.

CAPACITANCE ($Ta = 25\,°C$, $f = 1\,MHz$)

SYMBOL	PARAMETER	TEST CONOITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GNO	10	

Note : This parameter periodically sampled is not 100 % tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70 °C, V_{DD} = 5 V ± 10 %)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	-	100	-	ns
t_{ACC}	Address Access Time	-	85	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	85	-	100	
t_{CO2}	CE2 Access Time	-	85	-	100	
t_{OE}	Output Enable to Output in Valid	-	45	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	30	-	35	
t_{ODO}	Output Enable to Output in High-Z	-	30	-	35	
t_{OH}	Output Data Hold Time	10	-	10	-	

Write Cycle

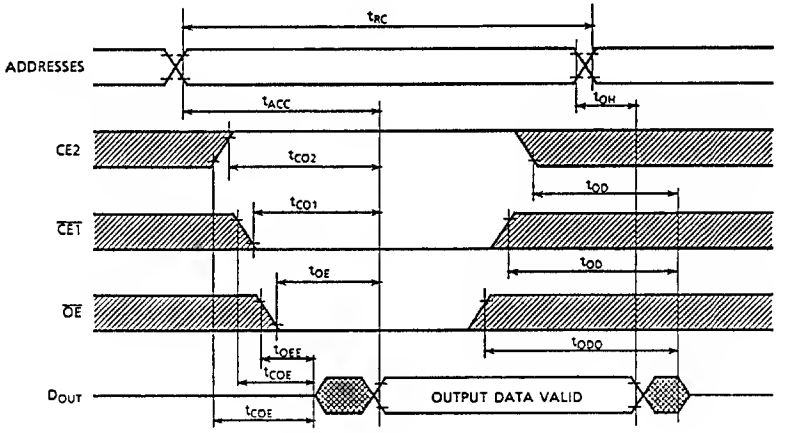
SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	-	100	-	ns
t_{WP}	Write Pulse Width	60	-	60	-	
t_{CW}	Chip Selection to End of Write	75	-	80	-	
t_{AS}	Address Set up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	R/W to Output in High-Z	-	30	-	35	
t_{OEW}	R/W to Output in Low-Z	0	-	0	-	
t_{DS}	Data Set up Time	35	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

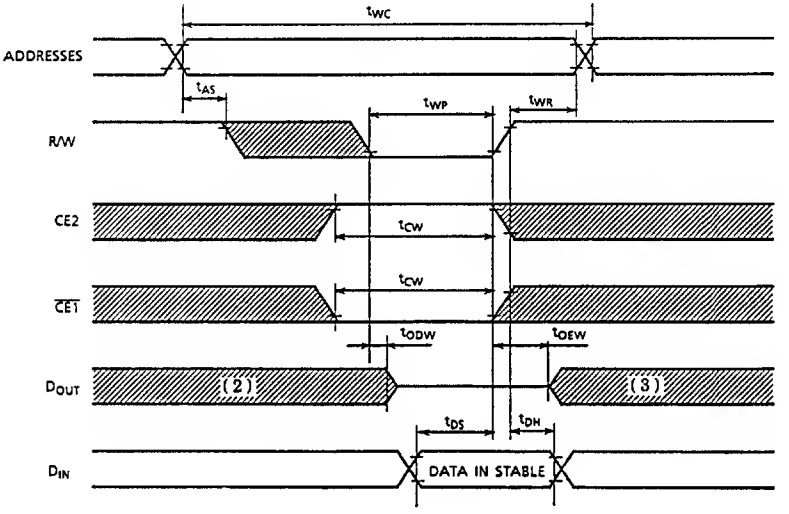
Output Load	:	100 pF + 1 TTL Gate
Input Pulse Level	:	0.6 V, 2.4 V
Timing Measurement V_{IN}	:	0.8 V, 2.2 V
Reference Level V_{OUT}	:	0.8 V, 2.2 V
t_r, t_f	:	5 ns

TIMING WAVEFROMS

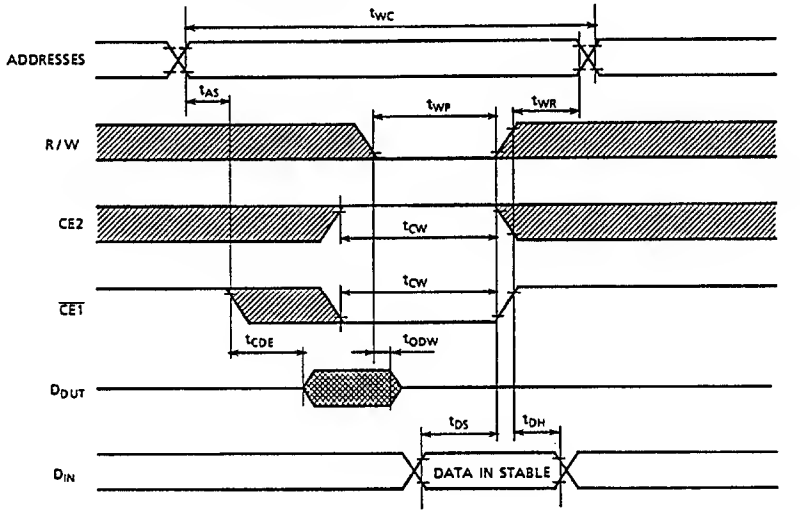
Read Cycle (1)



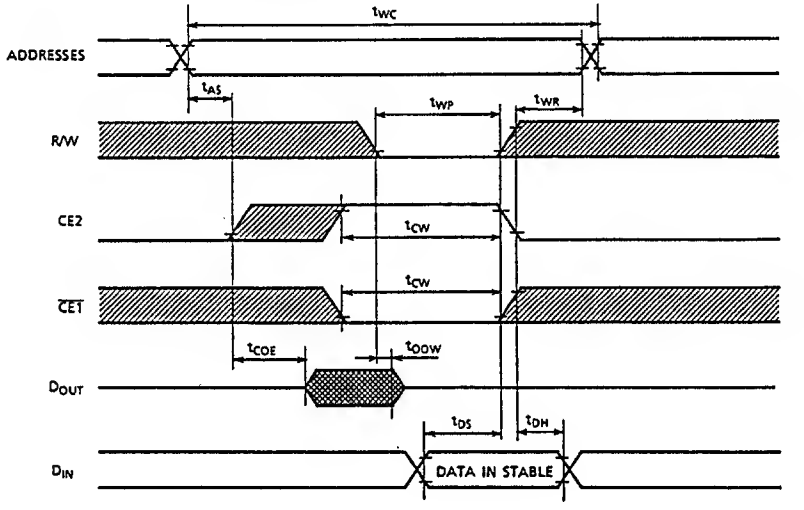
Write Cycle 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note : (1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

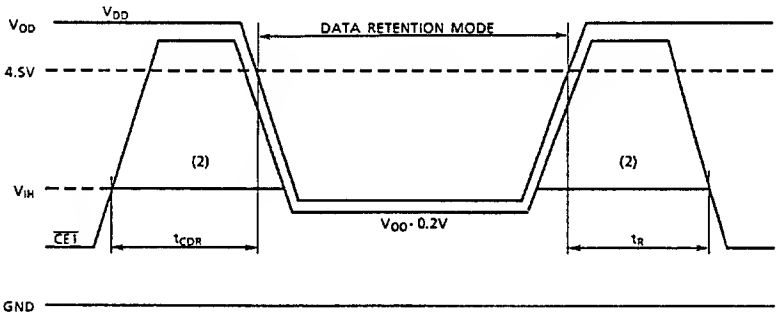
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

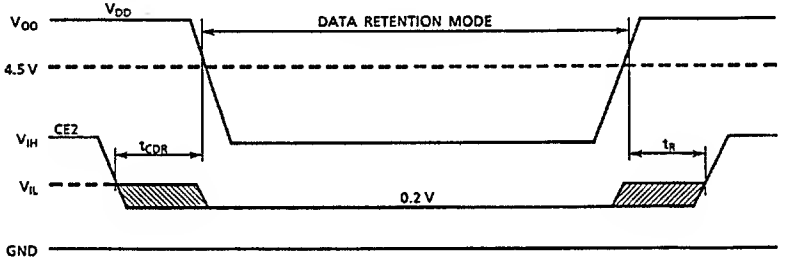
DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0 V	-	-	50	μA
		V_{DD} = 5.5 V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)

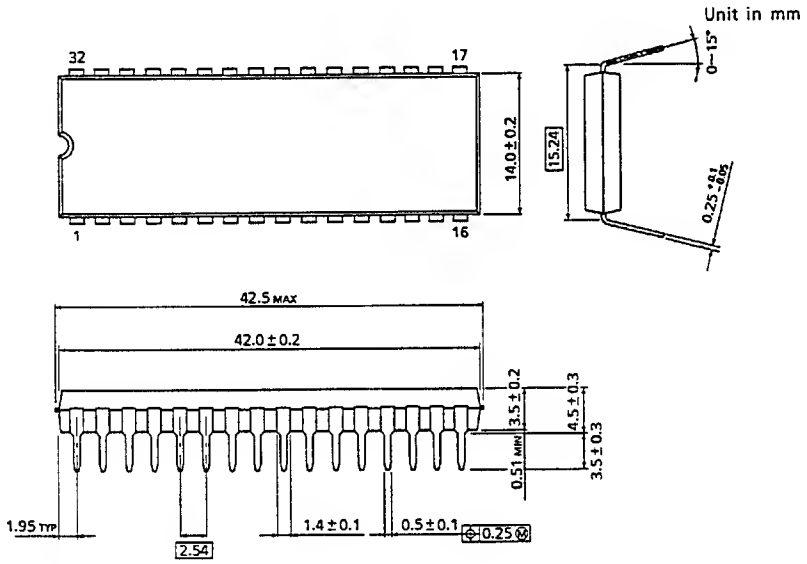


Note : (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2 V or CE2 ≧ V_{DD} − 0.2 V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2 V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4 V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2 V.

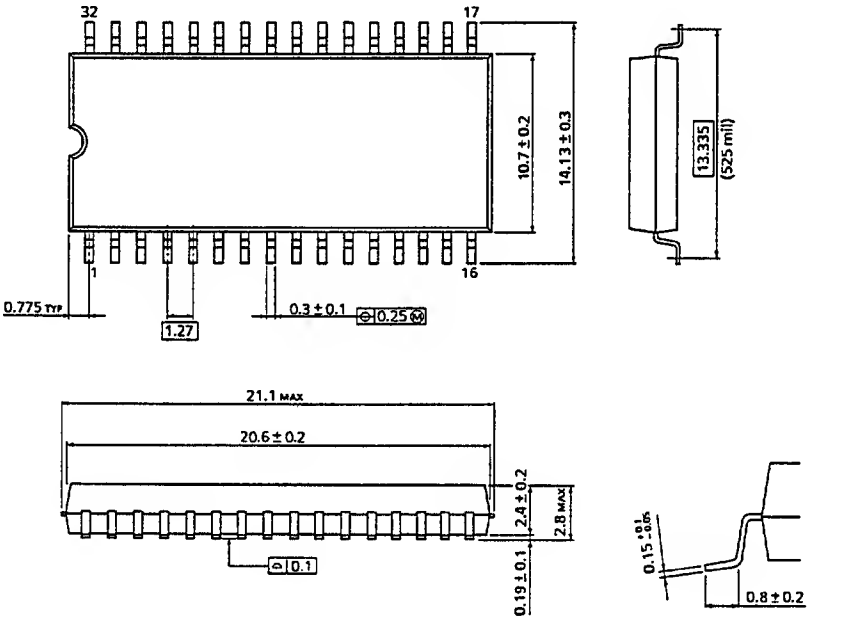
OUTLINE DRAWING (DIP32 - P - 600)



Weight : 4.53g (Typ.)

OUTLINE DRAWING (SOP32 - P - 525)

Unit in mm



Weight : 1.10g (Typ.)

131,072 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 85/100ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out-line plastic flat package.

FEATURES

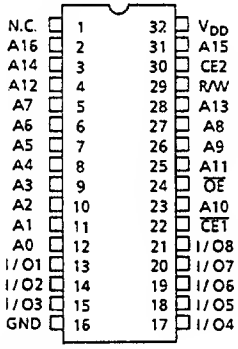
- Low Power Dissipation
  : 27.5mW/MHz (Typ.)
- Standby Current : 4μA at Ta=25°C(MAX)
- 5V Single Power Supply
- Power Down Feature: $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs

- Access Time

	TC551001 PL/FL-85L	TC551001 PL/FL-10L
Access Time (max.)	85ns	100ns
$\overline{CE1}$ Access Time (max.)	85ns	100ns
CE2 Access Time (max.)	85ns	100ns
$\overline{OE}$ Access Time (max.)	45ns	50ns

- Package : TC551001PL-L : DIP32-P-600
  TC551001FL-L : SOP32-P-525

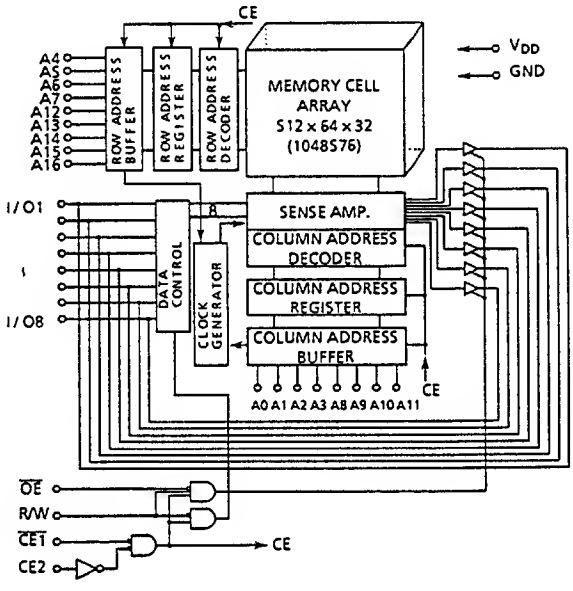
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power(+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3	−	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70\,°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/\overline{W} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/\overline{W} = V_{IH}$, $I_{OUT} = 0mA$, Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min. cycle		-	-	80	mA
I_{DDO2}		$\overline{CE1} = 0.2V$ and $CE2 = V_{DD} - 0.2V$, $R/\overline{W} = V_{DD} - 0.2V$, $I_{OUT} = 0mA$, Other Inputs = $V_{DD} - 0.2V/0.2V$, t_{cycle} = Min. cycle		-	-	70	mA
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$		-	-	3	mA
I_{DDS2} (1)		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$, $V_{DD} = 2.0V \sim 5.5V$	Ta = 25°C	-	2	4	μA
			Ta = 0~70°C	-	-	30	

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD} - 0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-85L TC551001FL-85L		TC551001PL-10L TC551001FL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	-	100	-	ns
t_{ACC}	Address Access Time	-	85	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	85	-	100	
t_{CO2}	CE2 Access Time	-	85	-	100	
t_{OE}	Output Enable to Output in Valid	-	45	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	30	-	35	
t_{ODO}	Output Enable to Output in High-Z	-	30	-	35	
t_{OH}	Output Data Hold Time	10	-	10	-	

Write Cycle

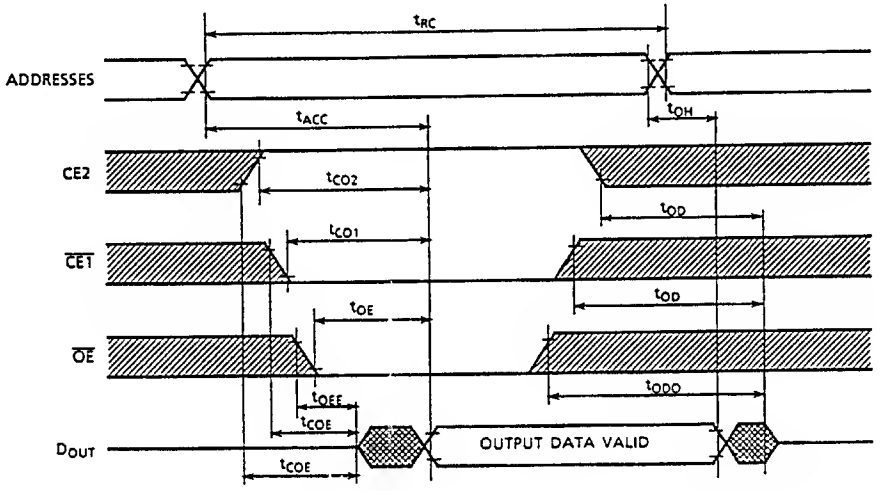
SYMBOL	PARAMETER	TC551001PL-85L TC551001FL-85L		TC551001PL-10L TC551001FL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	-	100	-	ns
t_{WP}	Write Pulse Width	60	-	60	-	
t_{CW}	Chip Selection to End of Write	75	-	80	-	
t_{AS}	Address Set up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	R/W to Output in High-Z	-	30	-	35	
t_{OEW}	R/W to Output in Low-Z	0	-	0	-	
t_{DS}	Data Set up Time	35	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

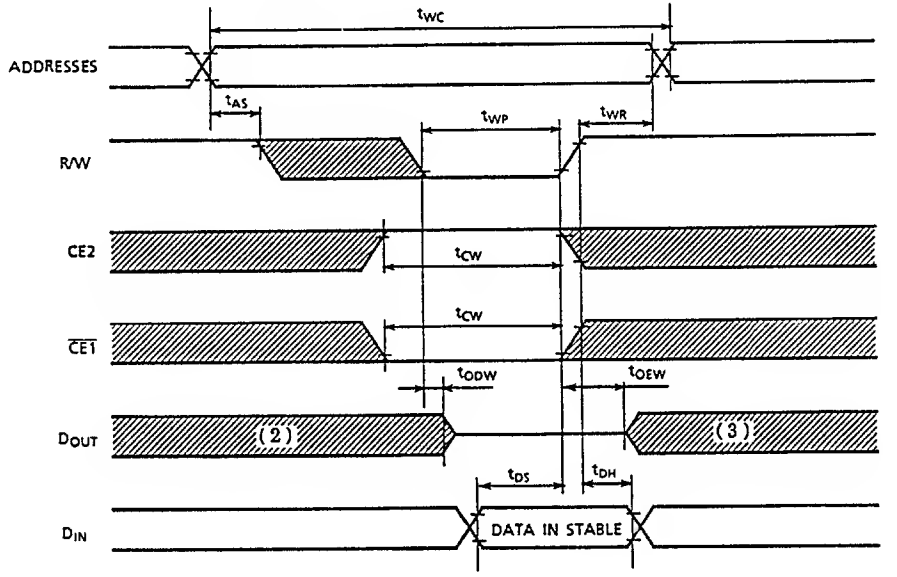
- Output Load : 100pF + 1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 0.8V, 2.2V
  Reference Level V_{OUT} : 0.8V, 2.2V
- t_r, t_f : 5ns

TIMING WAVEFORMS

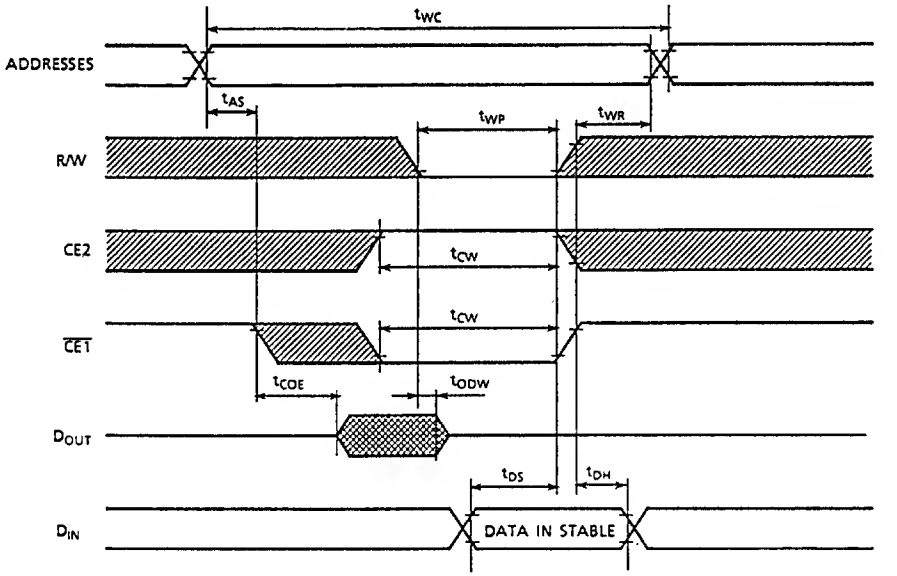
READ CYCLE (1)



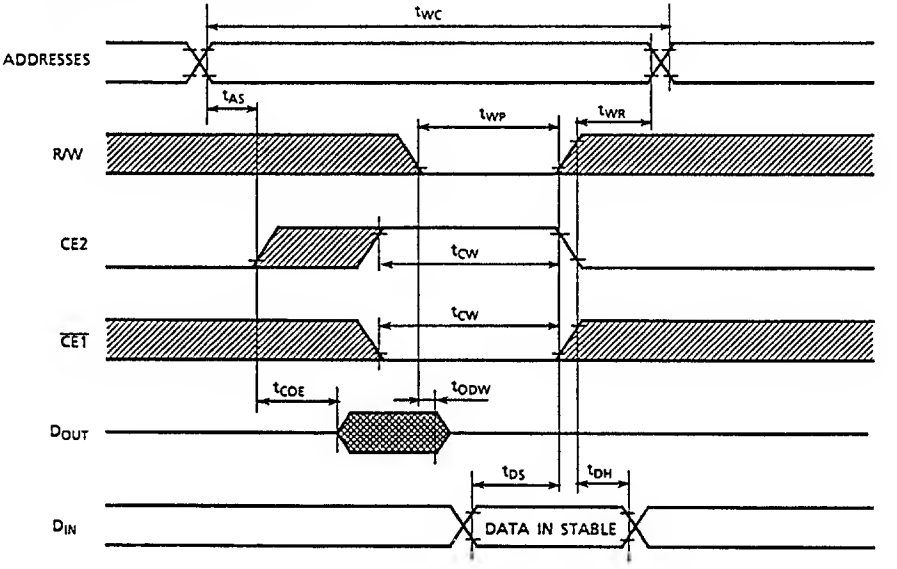
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

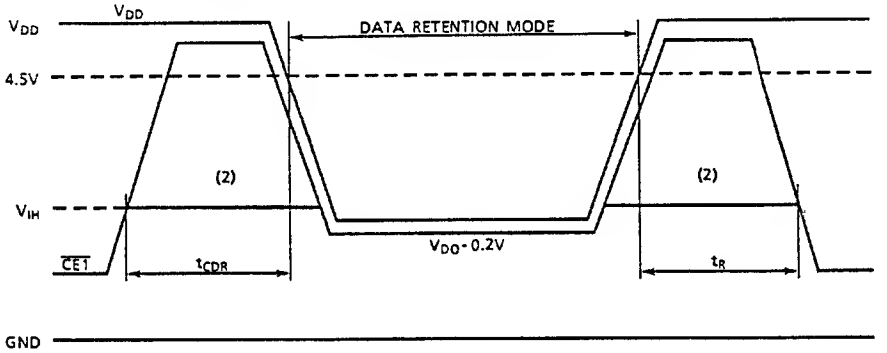
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

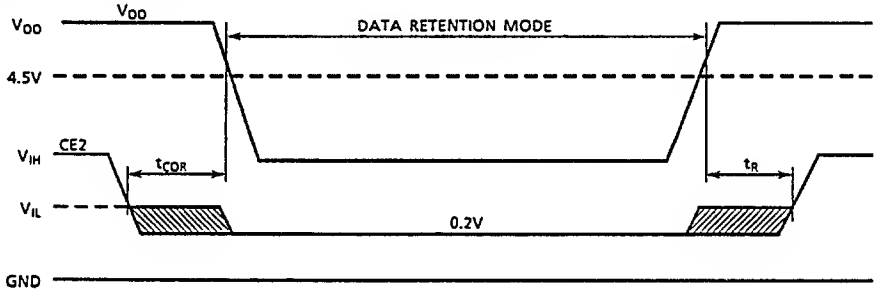
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	15*	μA
		V_{DD} = 5.5V	-	-	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

*) 3μA (MAX) at Ta = 0~40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

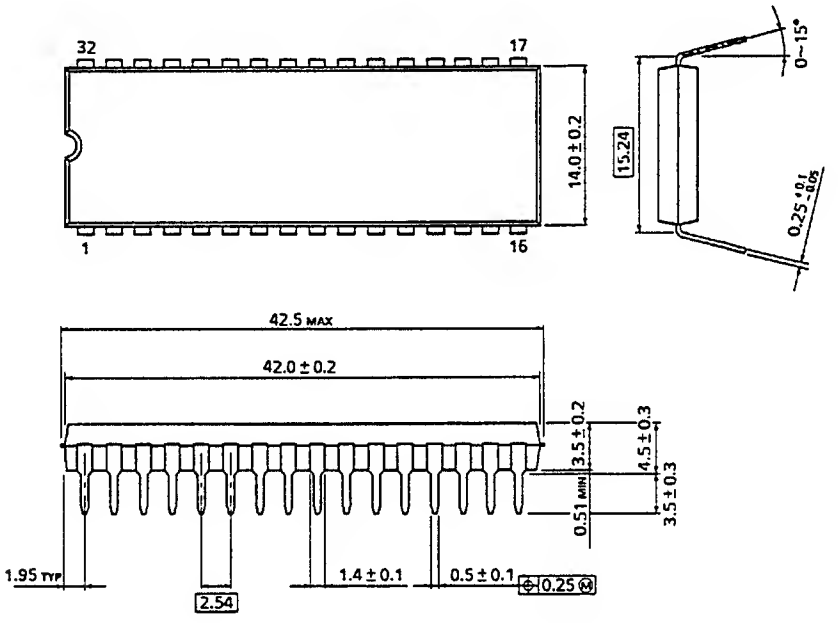
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32 – P – 600)

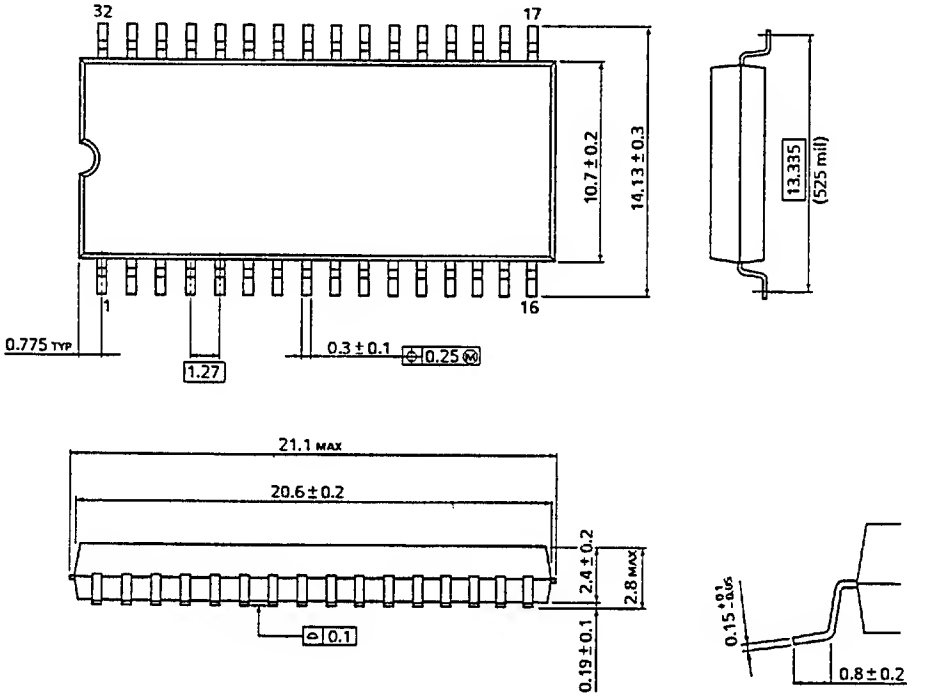
Unit in mm



Weight : 4.53g (Typ.)

OUTLINE DRAWING (SOP32 - P - 525)

Unit in mm



Weight : 1.10g (Typ.)

131,072 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC551001PI/FI is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 100ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001PI/FI has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PI/FI is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required. And TC551001PI/FI guarantees −40 ~ 85 °C operating temperature so TC551001PI/FI is suitable for use in wide operating temperature system.

The TC551001PI/FI is offered in both a dual-in-line 32 pin standard plastic package and small-out-line plastic flat package.

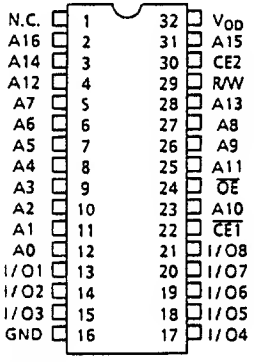
FEATURES

- Low Power Dissipation
  27.5mW/MHz (Typ.)
- Standby Current 4μA at Ta=25°C(MAX):
  TC551001PI-10L/FI-10L
- 5V Single Power Supply
- Power Down Feature: $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Wide Temperature Operating : −40 ~ 85 °C
- Access Time

Access Time (max.)	100ns
$\overline{CE1}$ Access Time (max.)	100ns
CE2 Access Time (max.)	100ns
$\overline{OE}$ Access Time (max.)	50ns

- Directly TTL Compatible: All Inputs and Outputs
- Package : TC551001PI-L : DIP32-P-600
  TC551001FI-L : SOP32-P-525

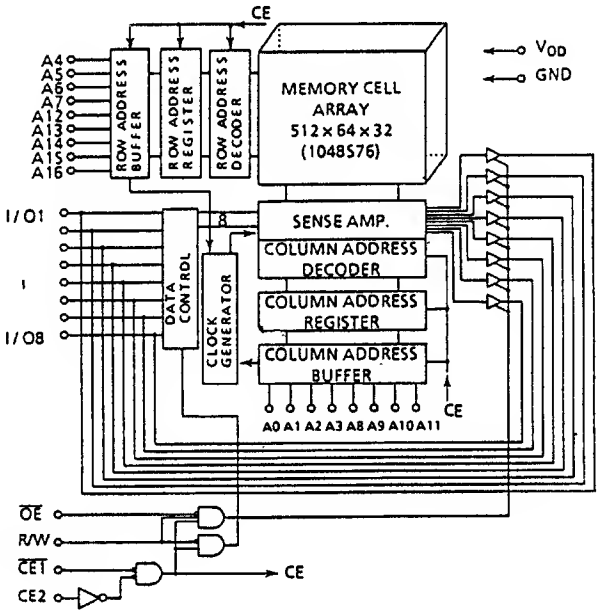
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	−40 ~ 85	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3	−	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

D.C. and OPERATING CHARACTERISTICS ($Ta = -40 \sim 85\,°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min. cycle		-	-	80	mA
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = $V_{DD}-0.2V$, R/W = $V_{DD}-0.2V$, I_{OUT} = 0mA, Other Inputs = $V_{DD}-0.2V$ / 0.2V, t_{cycle} = Min. cycle		-	-	70	mA
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or CE2 = V_{IL}		-	-	3	mA
I_{DDS2} (1)		$\overline{CE1} = V_{DD}-0.2V$ or CE2 = 0.2V, V_{DD} = 2.0V~5.5V	Ta = 25°C	-	2	4	μA
			Ta = -40~85°C	-	-	70	

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 $\geqq V_{DD}-0.2V$ or CE2 $\leqq 0.2V$.

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = -40 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC551001PI-10L TC551001FI-10L		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	ns
t_{ACC}	Address Access Time	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	100	
t_{CO2}	CE2 Access Time	-	100	
tOE	Output Enable to Output in Valid	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	40	
t_{ODO}	Output Enable to Output in High-Z	-	40	
t_{OH}	Output Data Hold Time	10	-	

Write Cycle

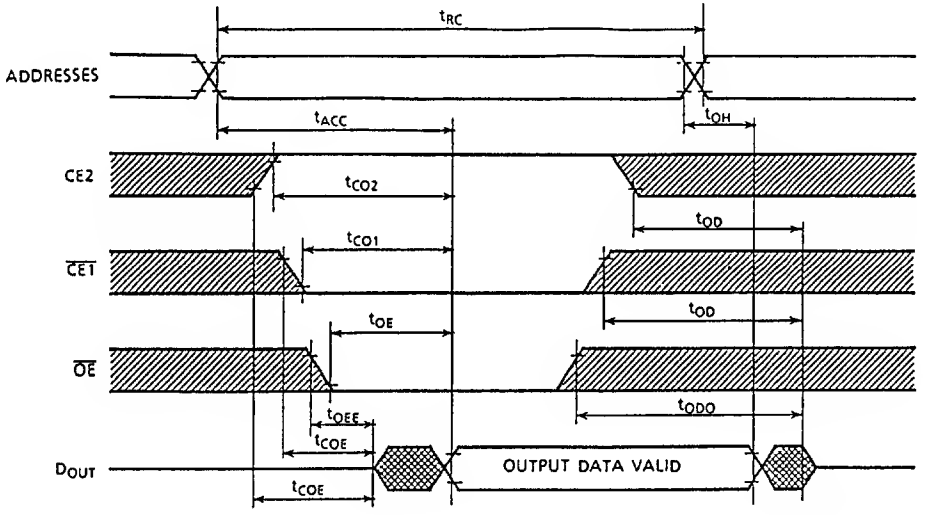
SYMBOL	PARAMETER	TC551001PI-10L TC551001FI-10L		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	ns
t_{WP}	Write Pulse Width	70	-	
t_{CW}	Chip Selection to End of Write	80	-	
t_{AS}	Address Set up Time	0	-	
t_{WR}	Write Recovery Time	0	-	
t_{ODW}	R/W to Output in High-Z	-	40	
t_{OEW}	R/W to Output in Low-Z	0	-	
t_{OS}	Data Set up Time	40	-	
t_{OH}	Data Hold Time	0	-	

A.C. TEST CONDIONS

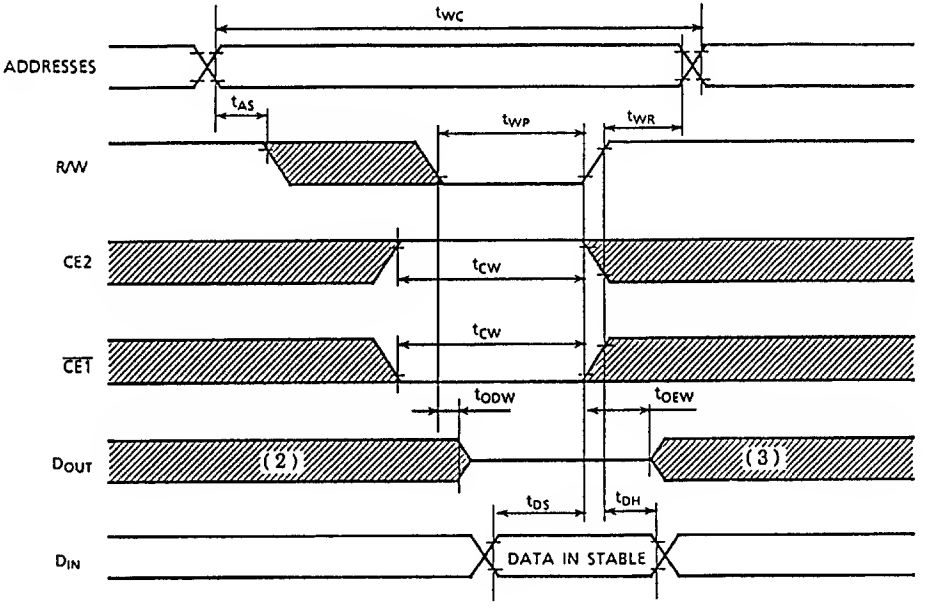
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.4V, 2.6V
- Timing Measurement V_{IN} : 0.6V, 2.4V
  Reference Level V_{OUT} : 0.8V, 2.2V
- t_r, t_f : 5ns

TIMING WAVEFORMS

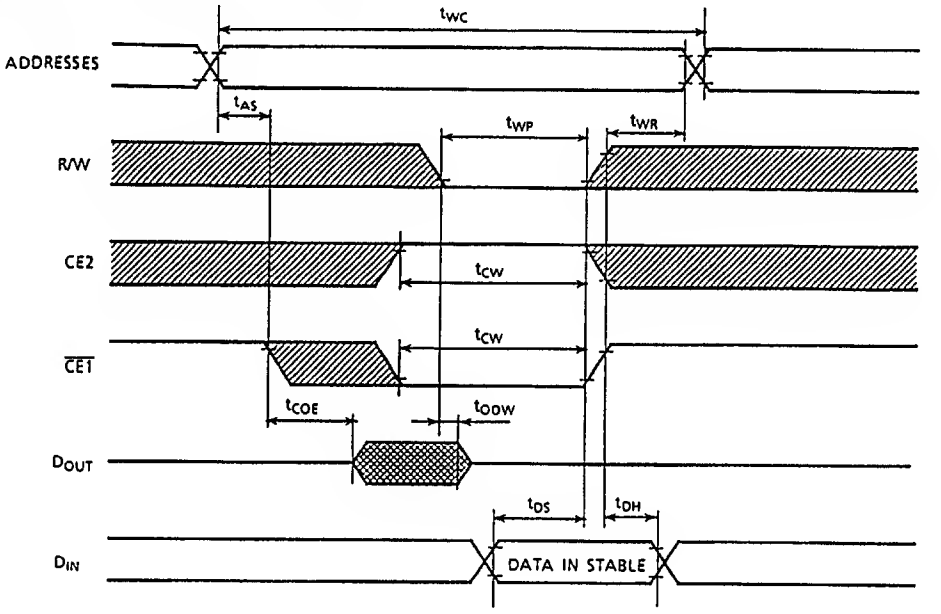
READ CYCLE (1)



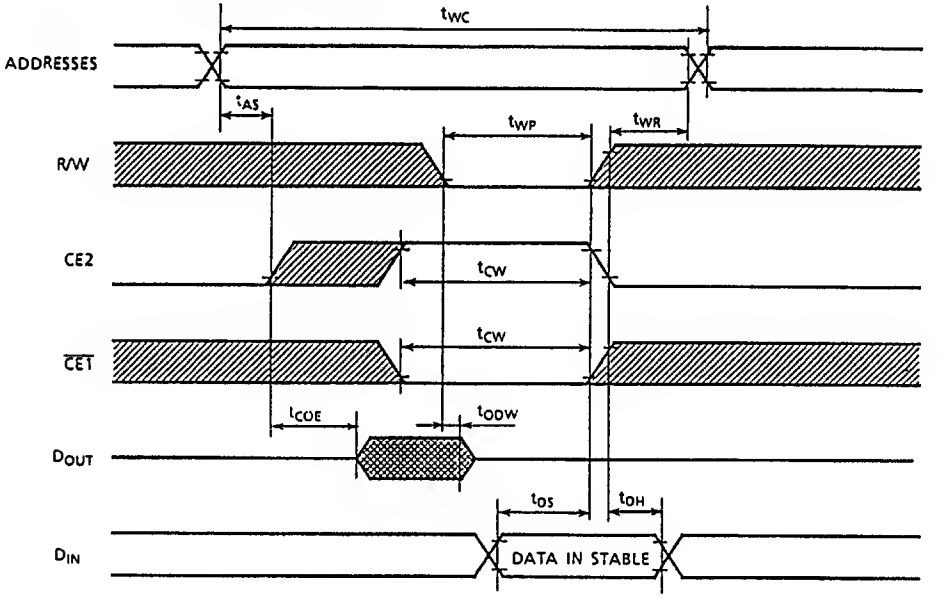
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

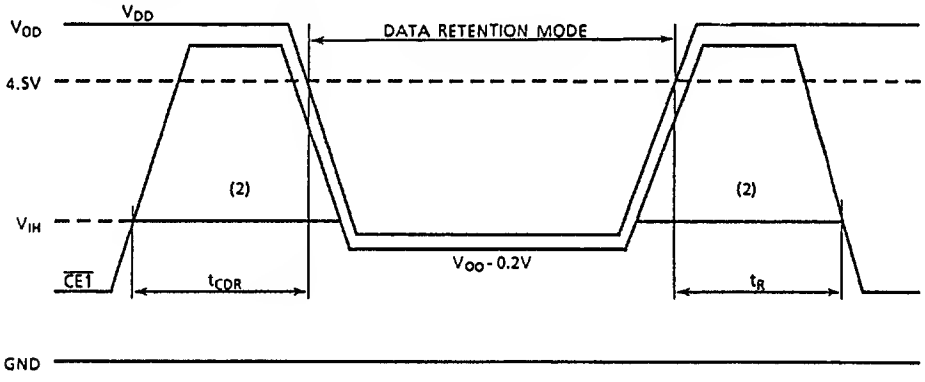
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = −40 ~ 85 °C)

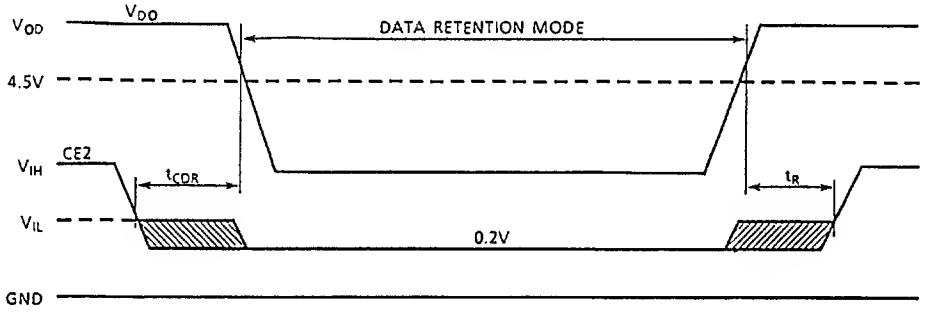
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	35*	μA
		V_{DD} = 5.5V	-	-	70	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

*) 3μA (MAX) at Ta = −40~40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

(1) In $\overline{CE1}$ controlled data retention mode, minmum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

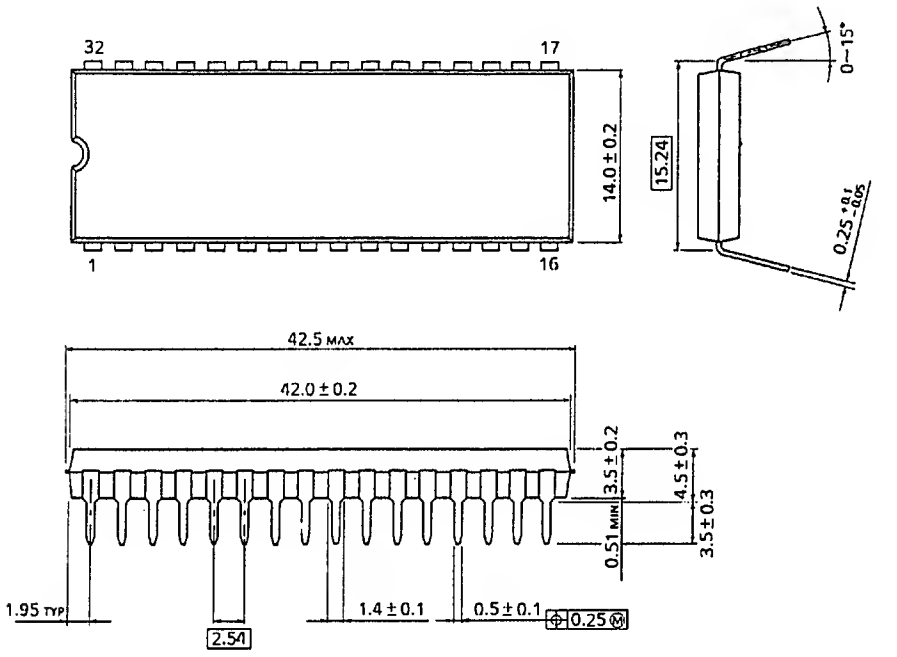
(2) If the V_{IH} of $\overline{CE1}$ is 2.4V in operaton, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING

(DIP32 - P - 600)

UNIT in mm

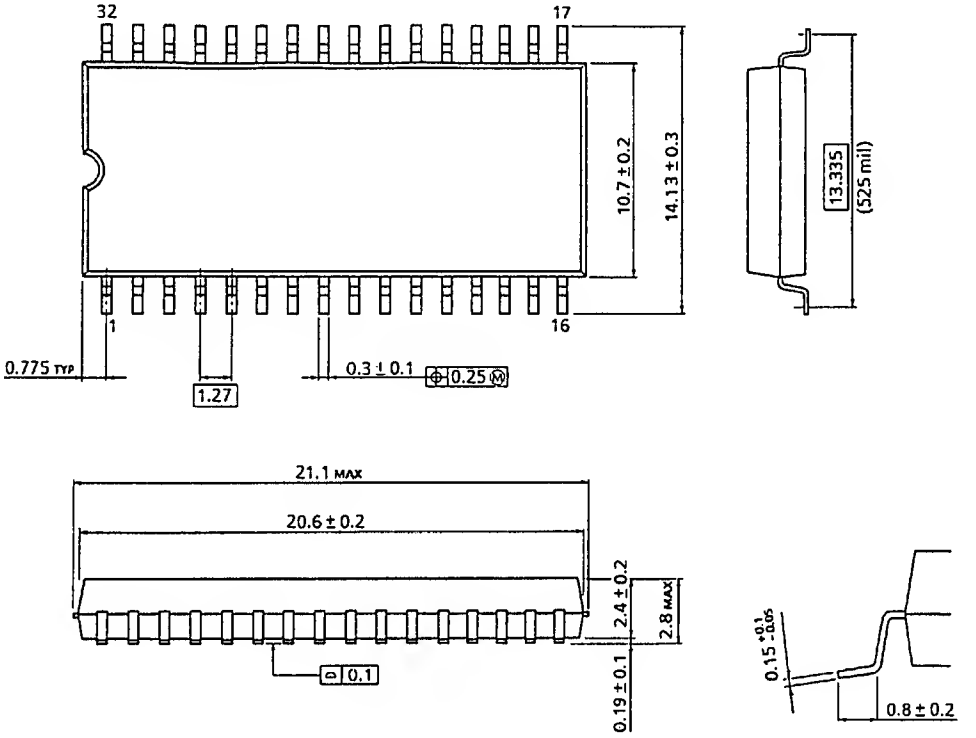


Weight : 4.53g (TYP.)

OUTLINE DRAWING

(SOP32 - P - 525)

UNIT in mm



Weight : 1.10g (TYP.)

131,072 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC551001APL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC551001APL is offered in a dual-in-line 32 pin standard plastic package, small-out-line plastic package and thin small-out-line plastic package (forward, reverse type).

FEATURES

- Low Power Dissipation
  : 27.5mW/MHz (Typ.) Operating
- Standby Current: 100μA (Max.)
- 5V Single Power Supply
- Power Down Features : $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs

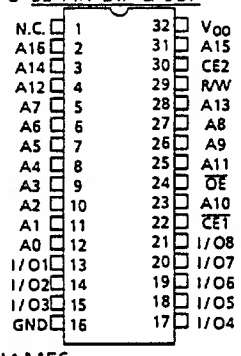
- Access Time (max.)

	TC551001APL/AFL/AFTL/ATRL-70	TC551001APL/AFL/AFTL/ATRL-85	TC551001APL/AFL/AFTL/ATRL-10
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
$\overline{OE}$ Access Time	35ns	45ns	50ns

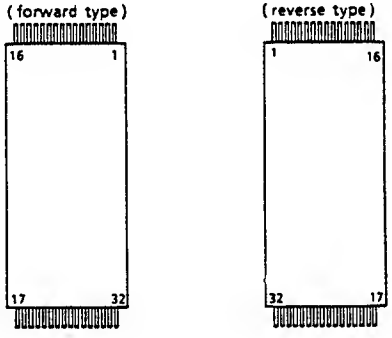
- Package : TC551001APL : DIP32-P-600
  TC551001AFL : SOP32-P-525
  TC551001AFTL : TSOP32-P-0820
  TC551001ATRL : TSOP32-P-0820A

PIN CONNECTION (TOP VIEW)

o 32 PIN DIP & SOP



o 32 PIN TSOP

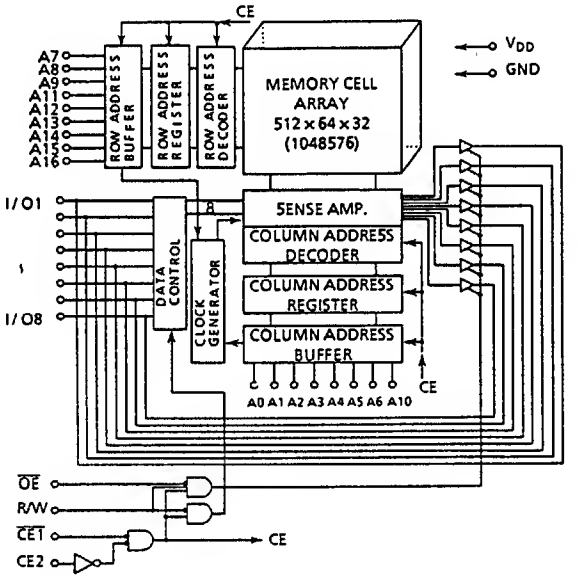


PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
VOO	Power (+5V)
GND	Ground
N.C.	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{OO}	N.C.	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CET}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0 / 0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	- 0.3	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70 °C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			-	-	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			- 1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			-	-	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	Min.	-	-	70	mA
				1 μs	-	-	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD}-0.2V R/W = V_{DD}-0.2V, I_{OUT} = 0mA Other Inputs = V_{DD}-0.2V/0.2V	Tcycle	Min.			60	mA
				1 μs	-	-	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			-	-	3	mA
I_{DDS2} (1)		$\overline{CE1}$ = V_{DD}-0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V, Ta = 0 ~ 70°C			-	2	100	μA

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD}-0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551001APL-70 TC551001AFL-70 TC551001AFTL-70 TC551001ATRL-70		TC551001APL-85 TC551001AFL-85 TC551001AFTL-85 TC551001ATRL-85		TC551001APL-10 TC551001AFL-10 TC551001AFTL-10 TC551001ATRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t_{ACC}	Address Access Time	–	70	–	85	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	–	100	
t_{CO2}	CE2 Access Time	–	70	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	–	35	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

WRITE CYCLE

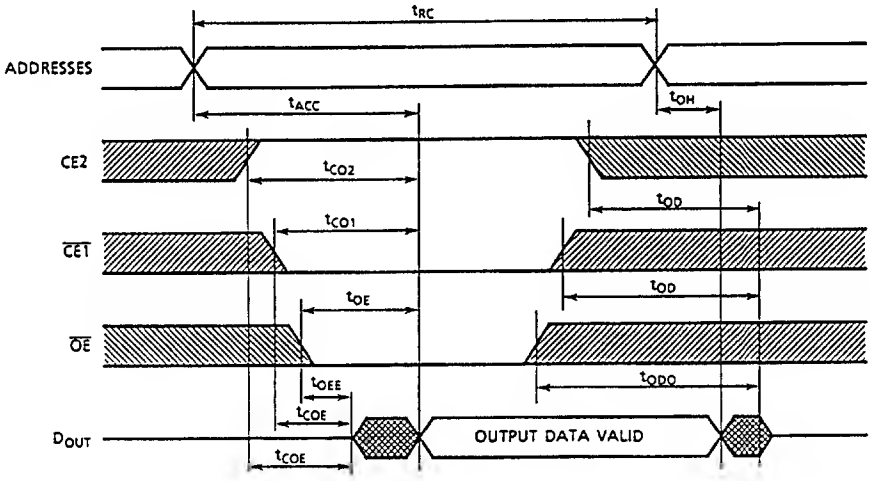
SYMBOL	PARAMETER	TC551001APL-70 TC551001AFL-70 TC551001AFTL-70 TC551001ATRL-70		TC551001APL-85 TC551001AFL-85 TC551001AFTL-85 TC551001ATRL-85		TC551001APL-10 TC551001AFL-10 TC551001AFTL-10 TC551001ATRL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	–	35	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

A.C. TEST CONDITIONS

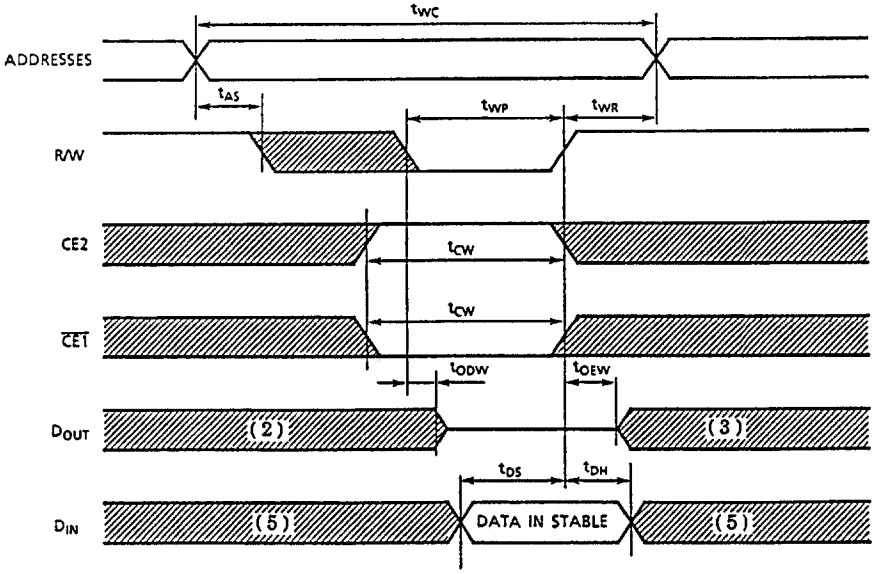
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

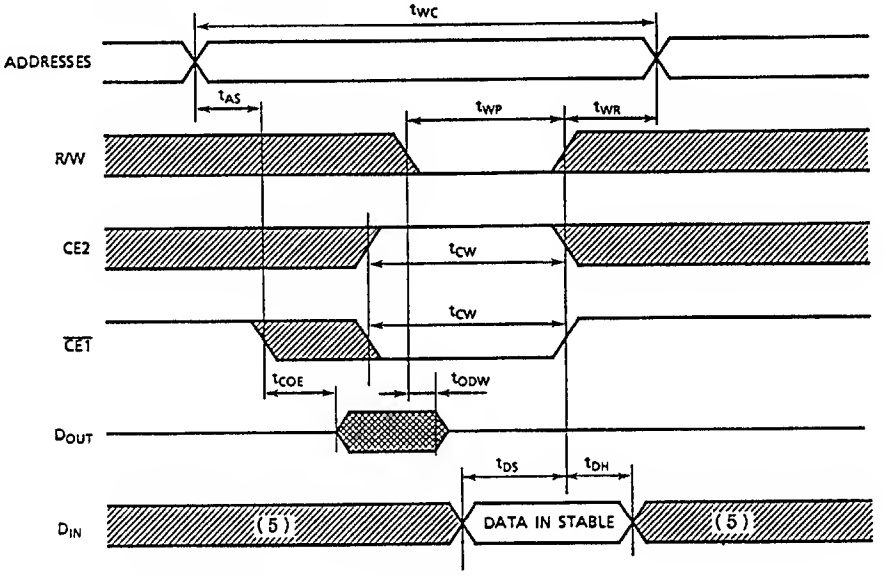
READ CYCLE (1)



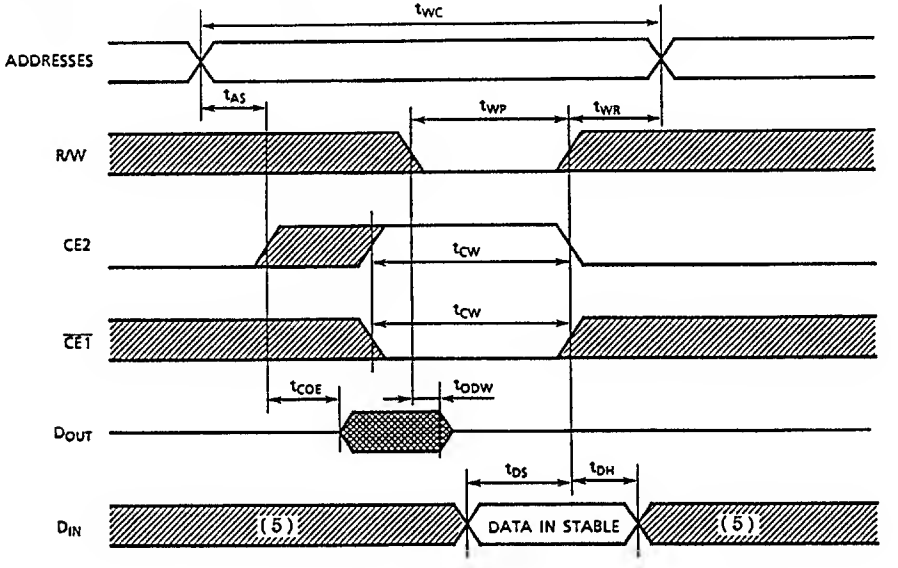
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

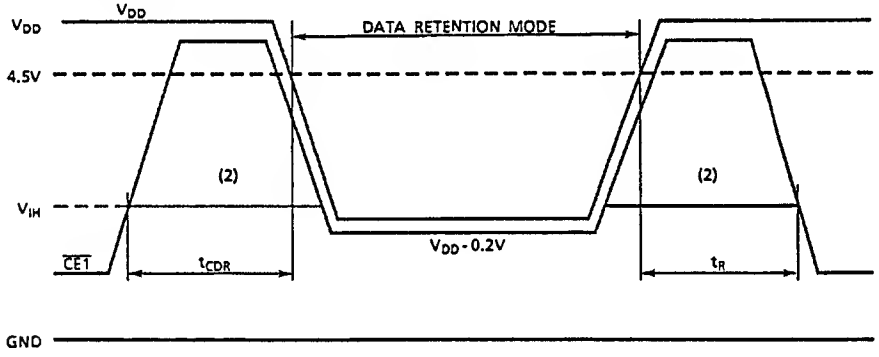
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

(5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

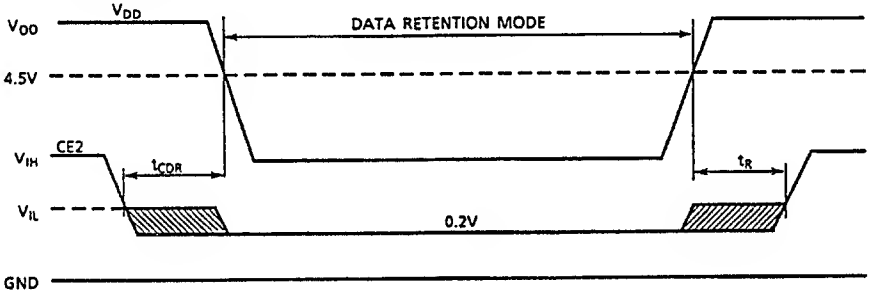
DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	50	μA
		V_{DD} = 5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

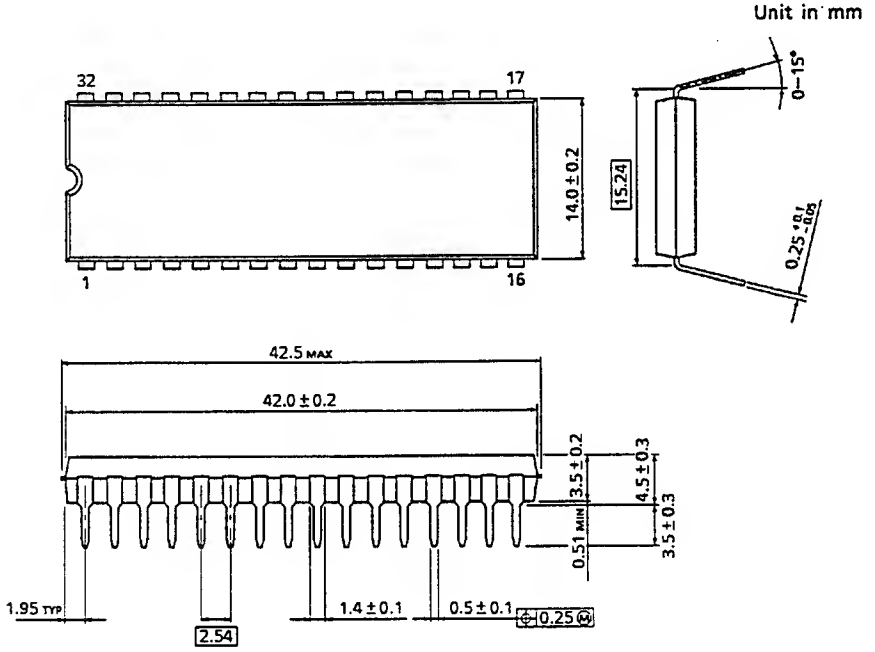
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32-P-600)

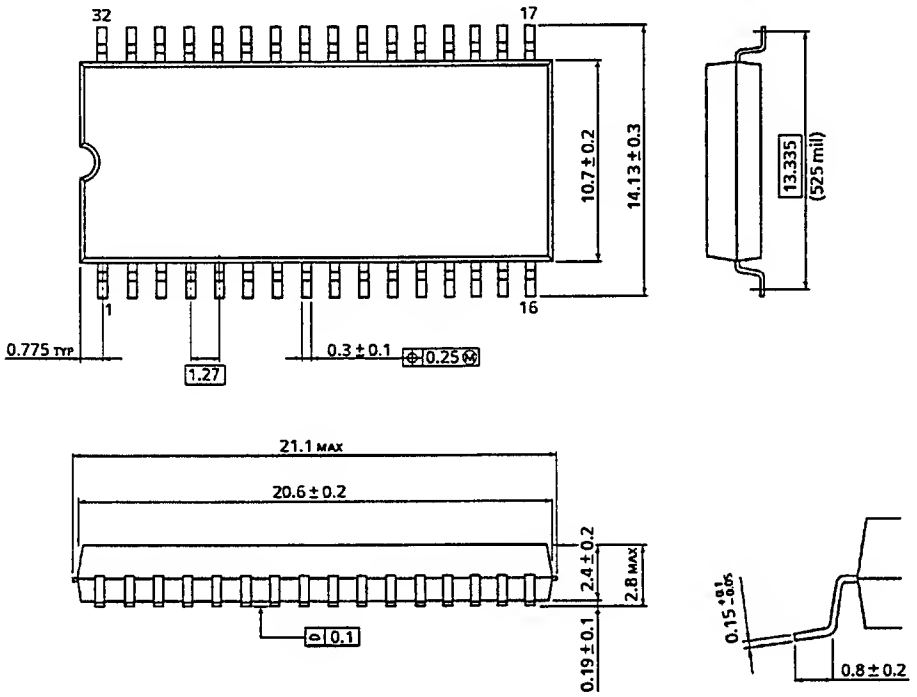
Unit in mm



Weight : 4.53 g (Typ.)

OUTLINE DRAWING (SOP32-P-525)

Unit in mm

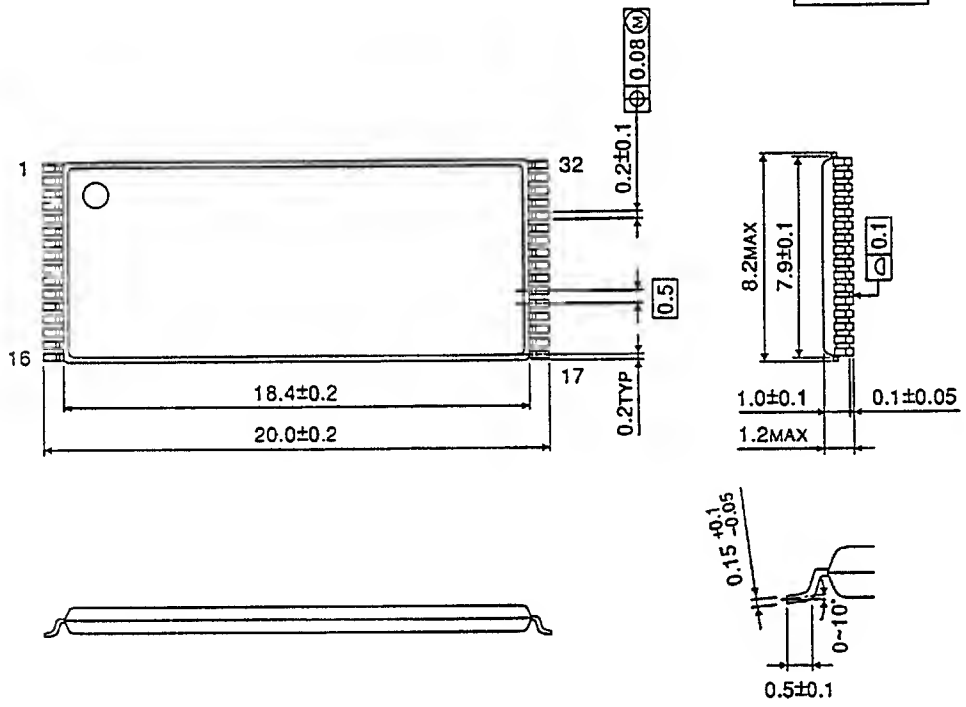


Weight : 1.10 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820)

Unit in mm

TENTATIVE

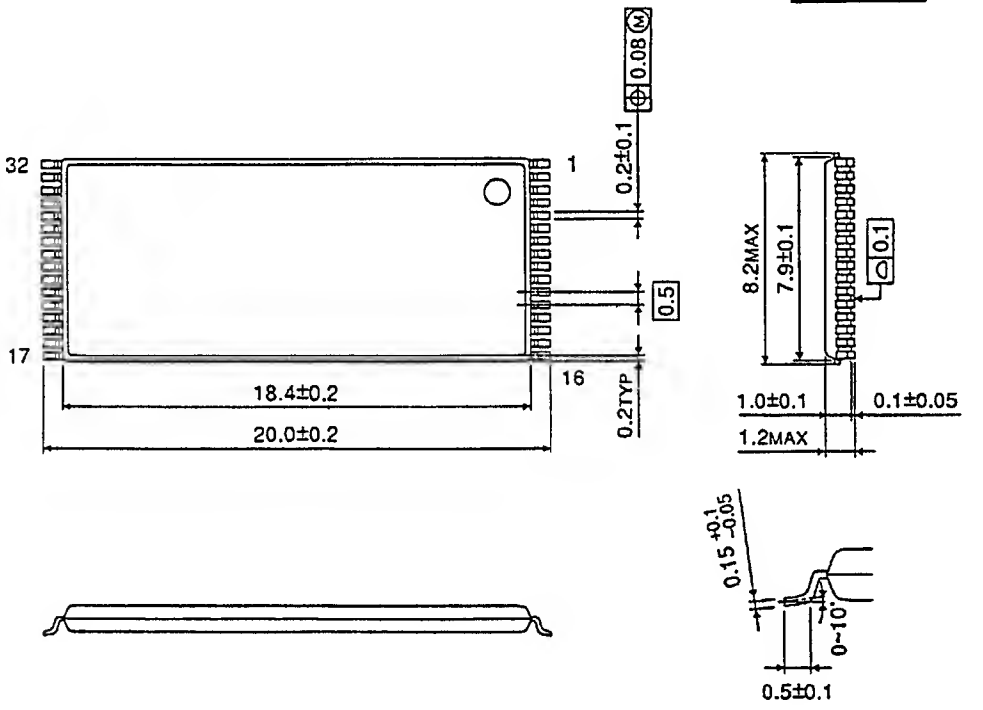


Weight : 0.36 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

131,072 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC551001APL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001APL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC551001APL is offered in a dual - in - line 32 pin standard plastic package, small - out - line plastic package and thin small - out - line plastic package (forward, reverse type).

FEATURES

- Low Power Dissipation
  : 27.5mW / MHz (Typ.) Operating
- Standby Current: 4μA (Max.) at Ta = 25°C
- 5V Single Power Supply
- Power Down Features : $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs

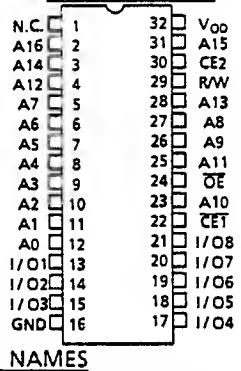
- Access Time (max.)

	TC551001APL/AFL/AFTL/ATRL-70	TC551001APL/AFL/AFTL/ATRL-85	TC551001APL/AFL/AFTL/ATRL-10
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
$\overline{OE}$ Access Time	35ns	45ns	50ns

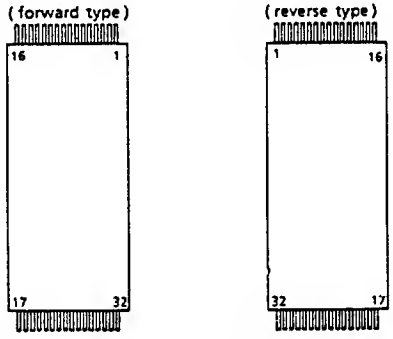
- Package : TC551001APL : DIP32-P-600
  TC551001AFL : SOP32-P-525
  TC551001AFTL : TSOP32-P-0820
  TC551001ATRL : TSOP32-P-0820A

PIN CONNECTION (TOP VIEW)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP

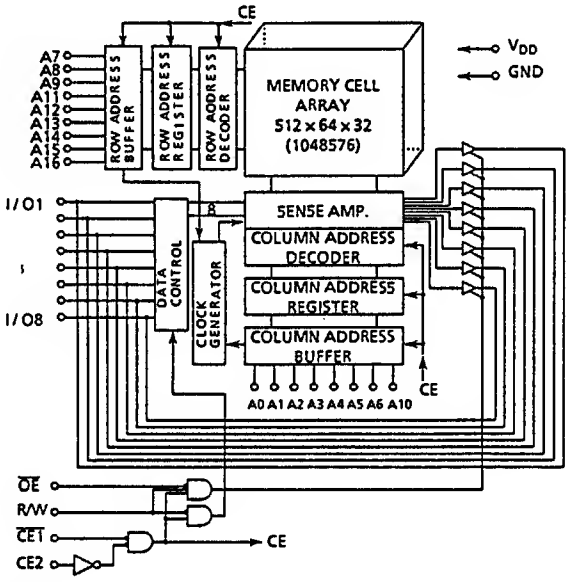


PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	N.C.	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DOO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70 °C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			-	-	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			-	-	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	Min.	-	-	70	mA
				1 μs	-	-	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD}-0.2V R/W = V_{DD}-0.2V, I_{OUT} = 0mA Other Inputs = V_{DD}-0.2V / 0.2V	Tcycle	Min.	-	-	60	mA
				1 μs	-	-	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			-	-	3	mA
I_{DDS2} (1)		$\overline{CE1}$ = V_{DD}-0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 25°C		-	2	4	μA
			Ta = 0 ~ 70°C		-	-	30	

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD}-0.2V or CE2 ≦ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551001APL-70L TC551001AFL-70L TC551001AFTL-70L TC551001ATRL-70L		TC551001APL-85L TC551001AFL-85L TC551001AFTL-85L TC551001ATRL-85L		TC551001APL-10L TC551001AFL-10L TC551001AFTL-10L TC551001ATRL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	-	85	-	100	-	ns
t_{ACC}	Address Access Time	-	70	-	85	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	70	-	85	-	100	
t_{CO2}	CE2 Access Time	-	70	-	85	-	100	
t_{OE}	Output Enable to Output in Valid	-	35	-	45	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	25	-	30	-	35	
t_{ODO}	Output Enable to Output in High-Z	-	25	-	30	-	35	
t_{OH}	Output Data Hold Time	10	-	10	-	10	-	

WRITE CYCLE

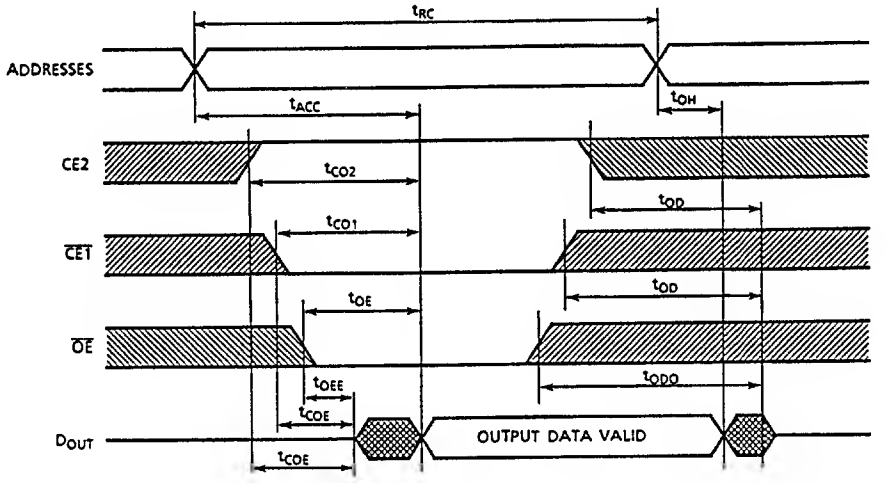
SYMBOL	PARAMETER	TC551001APL-70L TC551001AFL-70L TC551001AFTL-70L TC551001ATRL-70L		TC551001APL-85L TC551001AFL-85L TC551001AFTL-85L TC551001ATRL-85L		TC551001APL-10L TC551001AFL-10L TC551001AFTL-10L TC551001ATRL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t_{WP}	Write Pulse Width	50	-	60	-	60	-	
t_{CW}	Chip Selection to End of Write	60	-	75	-	80	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output in High-Z	-	25	-	30	-	35	
t_{OEW}	R/W to Output in Low-Z	5	-	5	-	5	-	
t_{DS}	Data Set up Time	30	-	35	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

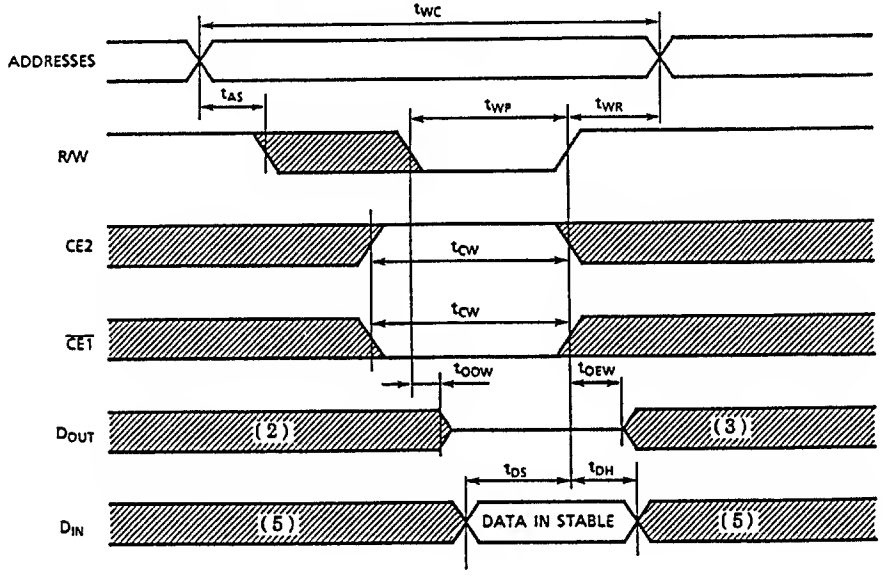
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

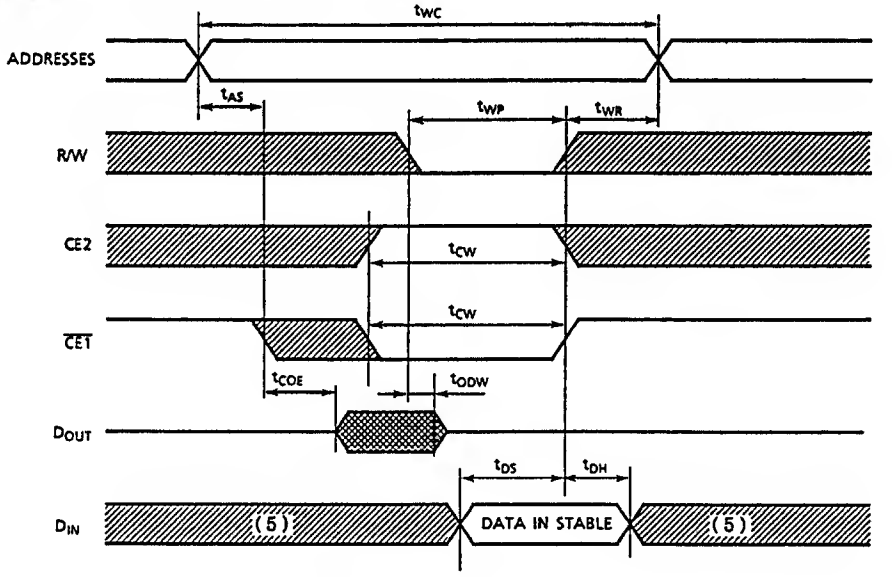
READ CYCLE (1)



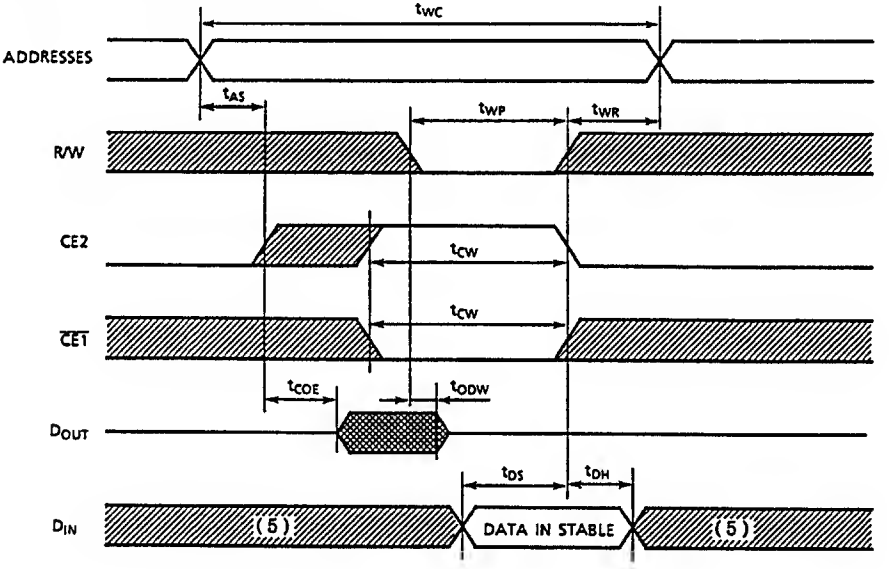
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE :

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

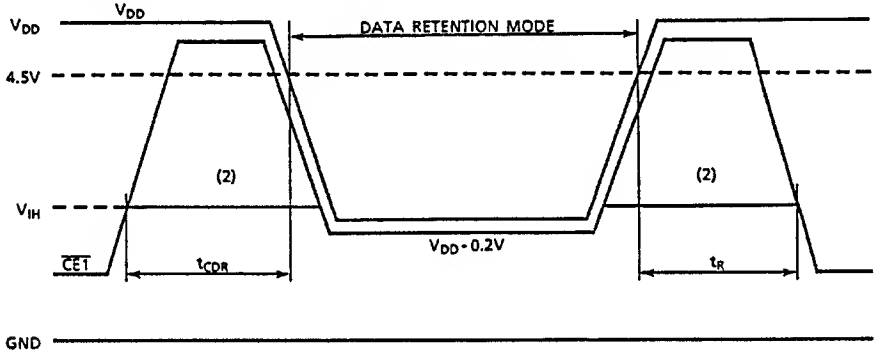
(5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

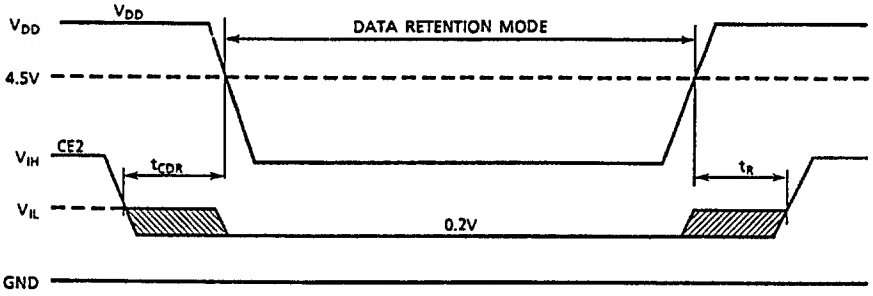
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	15*	μA
		V_{DD} = 5.5V	-	-	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

*) 3μA (MAX.) Ta = 0 ~ 40 °C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

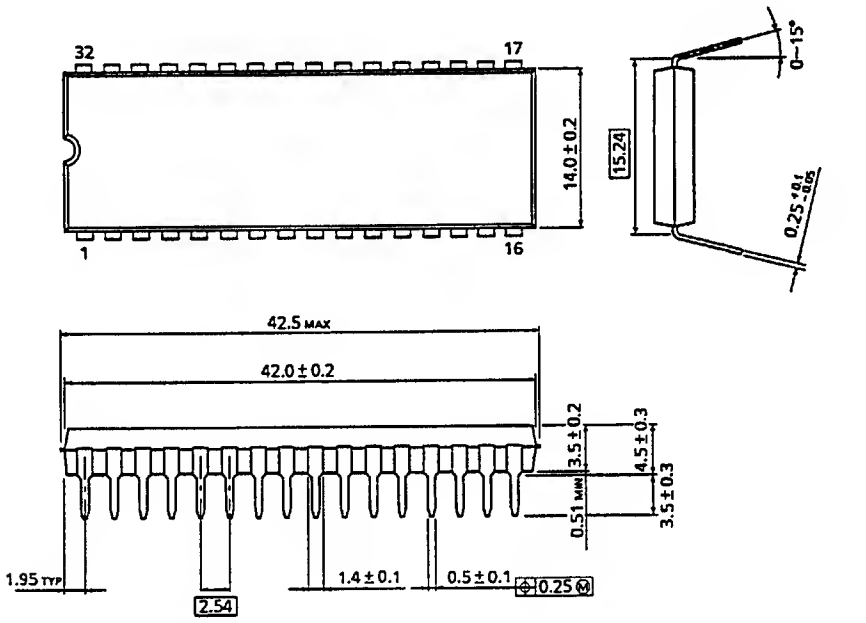
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32-P-600)

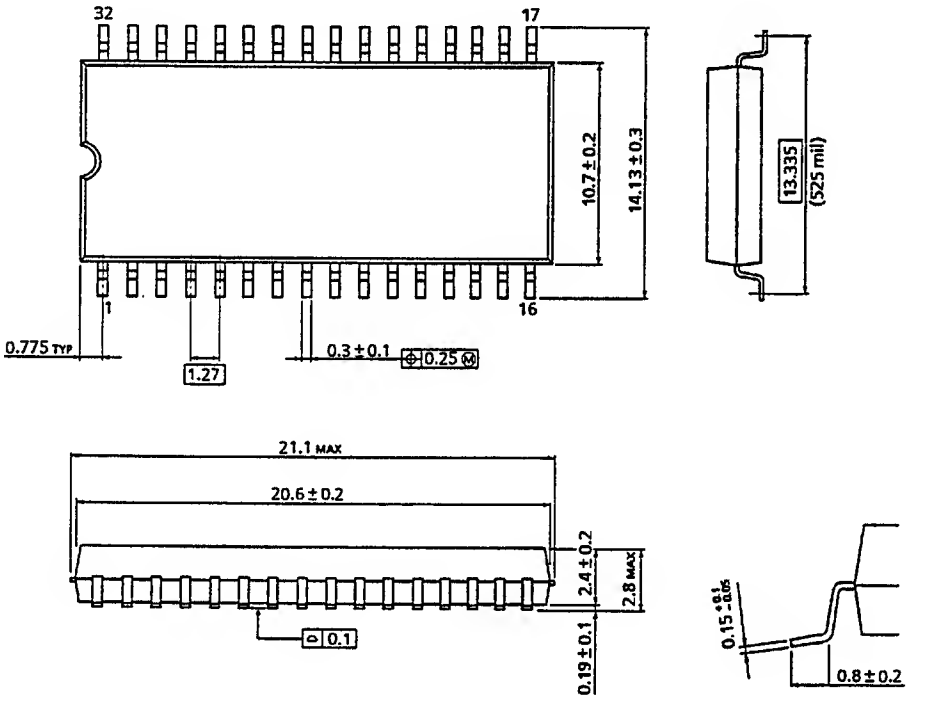
Unit in mm



Weight : 4.53 g (Typ.)

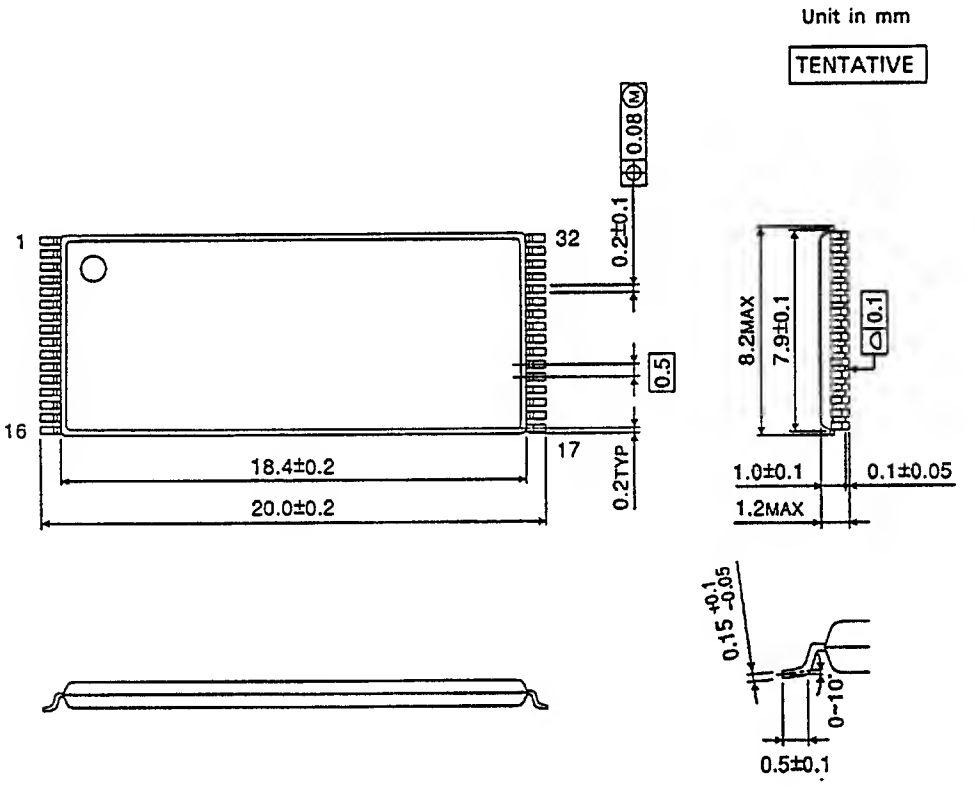
OUTLINE DRAWING (SOP32-P-525)

Unit in mm



Weight : 1.10 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820)

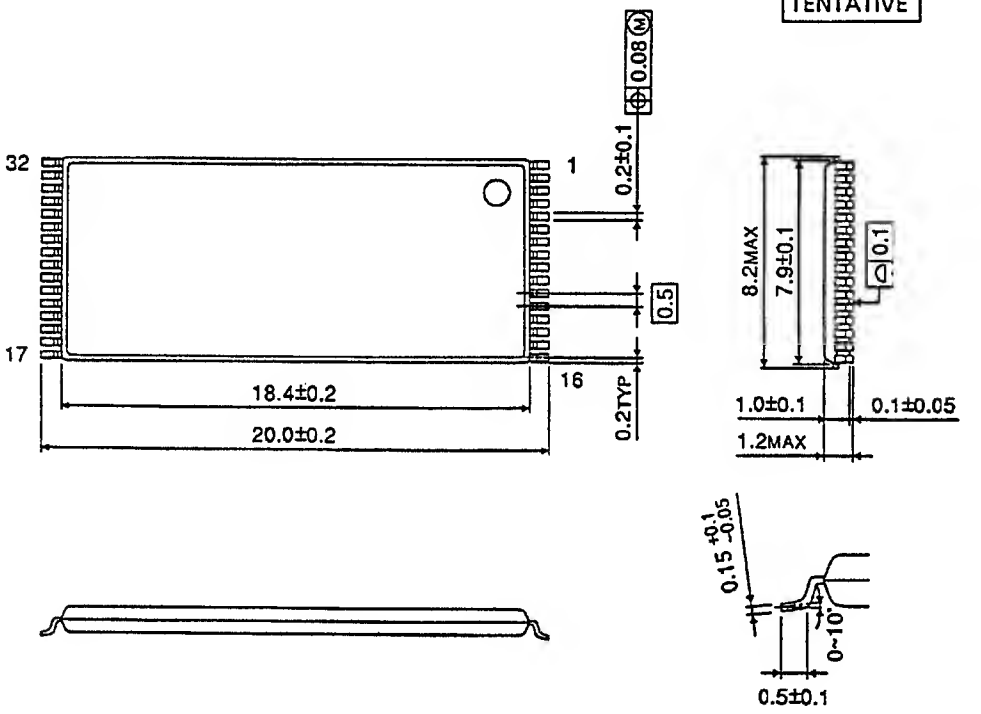


Weight : 0.36 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

131,072 WORDS × 8 BIT STATIC RAM

PRELIMINARY.

DESCRIPTION

The TC551001API is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 100ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001API has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001API is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. And TC551001API guarantees −40 ~ 85 °C operating temperature so TC551001API is suitable for use in wide operating temperature system.

The TC551001API is offered in a dual-in-line 32 pin standard plastic package, small-out-line plastic package and thin small-out-line plastic package (forward, reverse type).

FEATURES

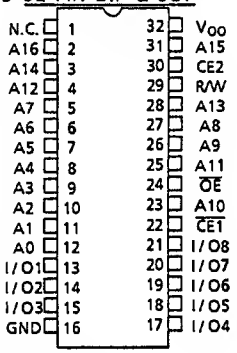
- Low Power Dissipation
  27.5mW/MHz (Typ.) Operating
- Standby Current: 200μA (Max.)
- 5V Single Power Supply
- Power Down Features : $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Wide Temperature Operating : −40~85 °C
- Access Time (max.)

Access Time	100ns
$\overline{CE1}$ Access Time	100ns
CE2 Access Time	100ns
$\overline{OE}$ Access Time	50ns

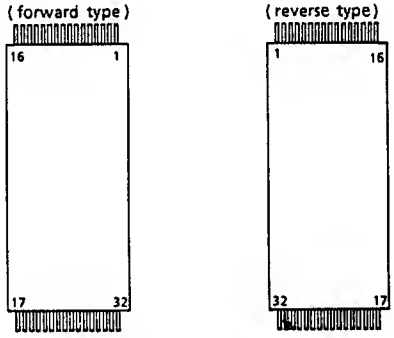
- Package
  TC551001API : DIP32-P-600
  TC551001AFI : SOP32-P-525
  TC551001AFTI : TSOP32-P-0820
  TC551001ATRI : TSOP32-P-0820A

PIN CONNECTION (TOP VIEW)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP

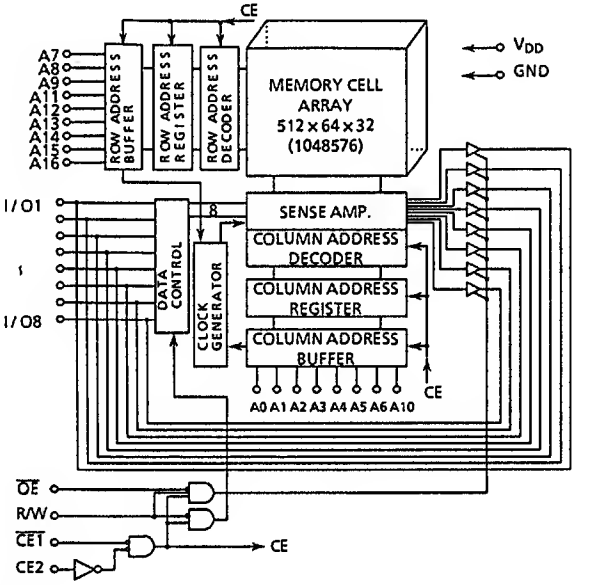


PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{OO}	Power (+5V)
GND	Ground
N.C.	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{OO}	N.C.	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	−40 ~ 85	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = −40 ~ 85 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3	−	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85 °C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			−	−	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			−	−	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	Min.	−	−	70	mA
				1 μs	−	−	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD}−0.2V R/W = V_{DD}−0.2V, I_{OUT} = 0mA Other Inputs = V_{DD}−0.2V/0.2V	Tcycle	Min.			60	mA
				1 μs	−	−	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			−	−	3	mA
I_{DDS2} (1)		$\overline{CE1}$ = V_{DD}−0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V, Ta = −40 ~ 85 °C			−	2	200	μA

Note: (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 $\geqq$ V_{DD}−0.2V or CE2 $\leqq$ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MIN.	UNIT
t_{RC}	Read Cycle Time	100	–	ns
t_{ACC}	Address Access Time	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	100	
t_{CO2}	CE2 Access Time	–	100	
t_{OE}	Output Enable to Output in Valid	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	40	
t_{ODO}	Output Enable to Output in High-Z	–	40	
t_{OH}	Output Data Hold Time	10	–	

WRITE CYCLE

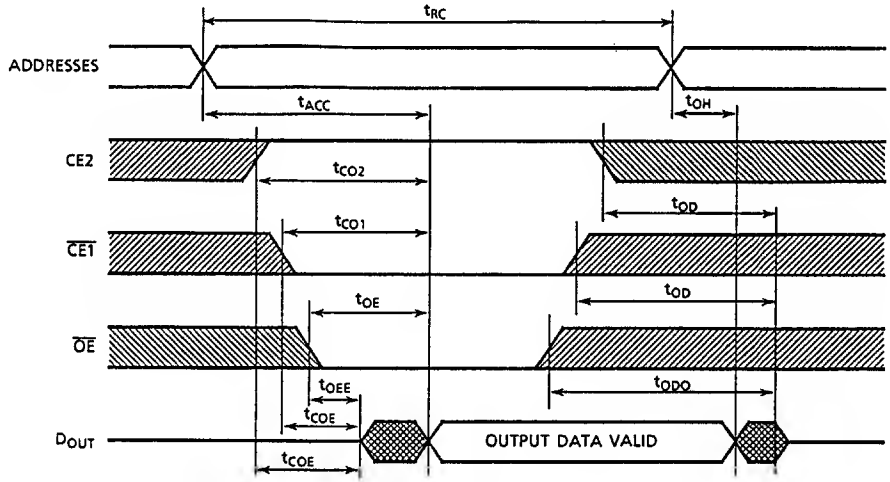
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	100	–	ns
t_{WP}	Write Pulse Width	60	–	
t_{CW}	Chip Selection to End of Write	80	–	
t_{AS}	Address Set up Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{OOW}	R/W to Output in High-Z	–	40	
t_{OEW}	R/W to Output in Low-Z	0	–	
t_{OS}	Data Set up Time	40	–	
t_{OH}	Data Hold Time	0	–	

A.C. TEST CONDITIONS

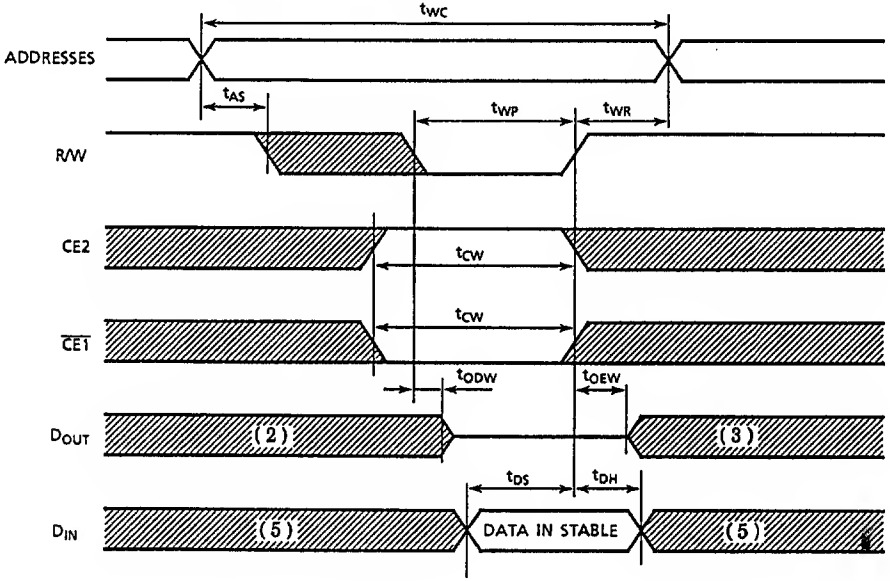
- Output Load : 100pF + 1 TTL Gate
- Input Pulse Level : 0.4V, 2.6V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

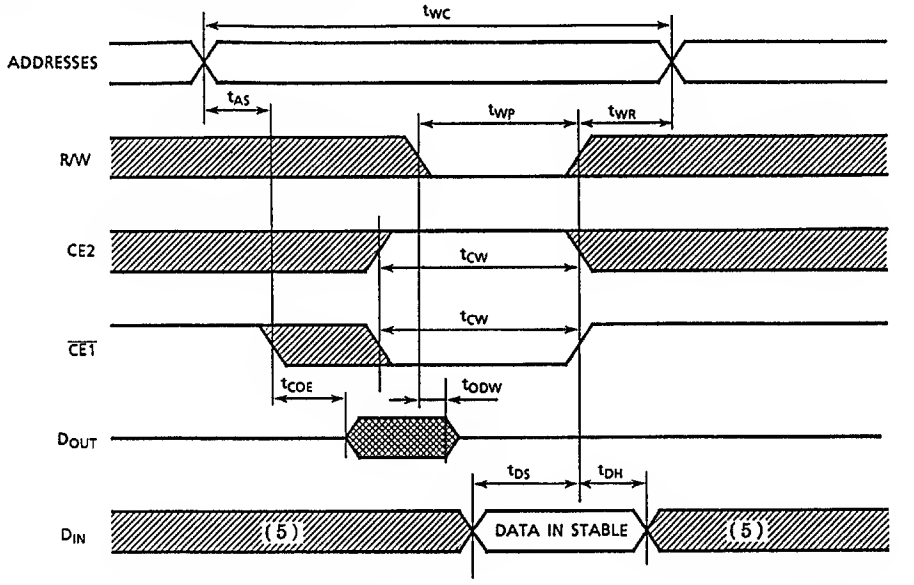
READ CYCLE (1)



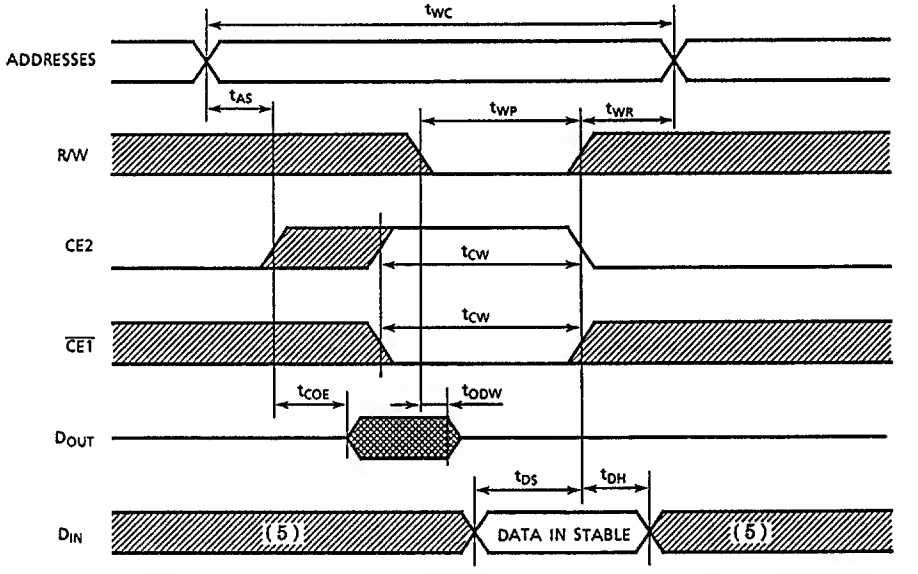
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

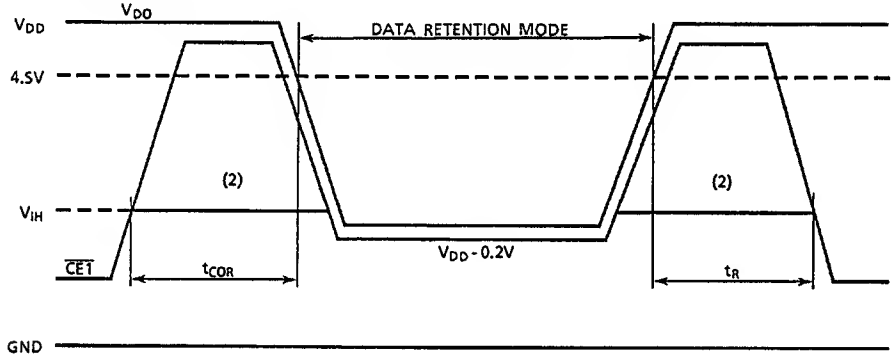
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

(5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

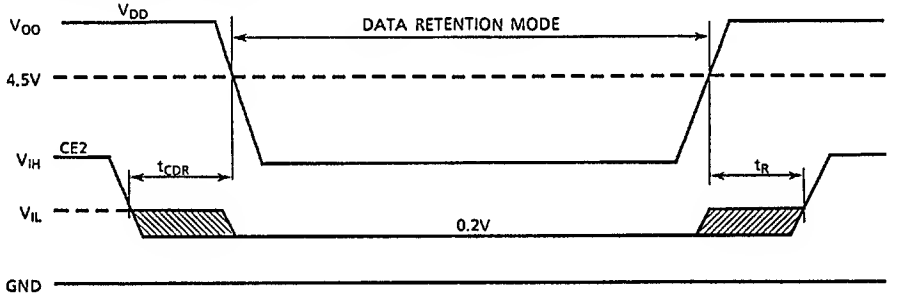
DATA RETENTION CHARACTERISTICS (Ta = -40 ~ 85 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	S.S	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	100	μA
		V_{DD} = S.SV	-	-	200	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		S	-	-	mS

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

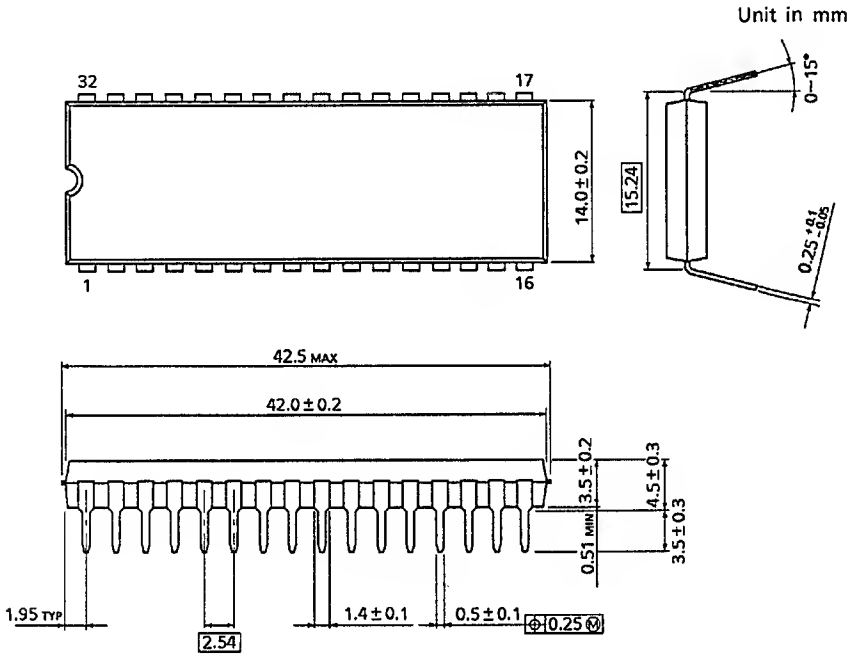
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32-P-600)

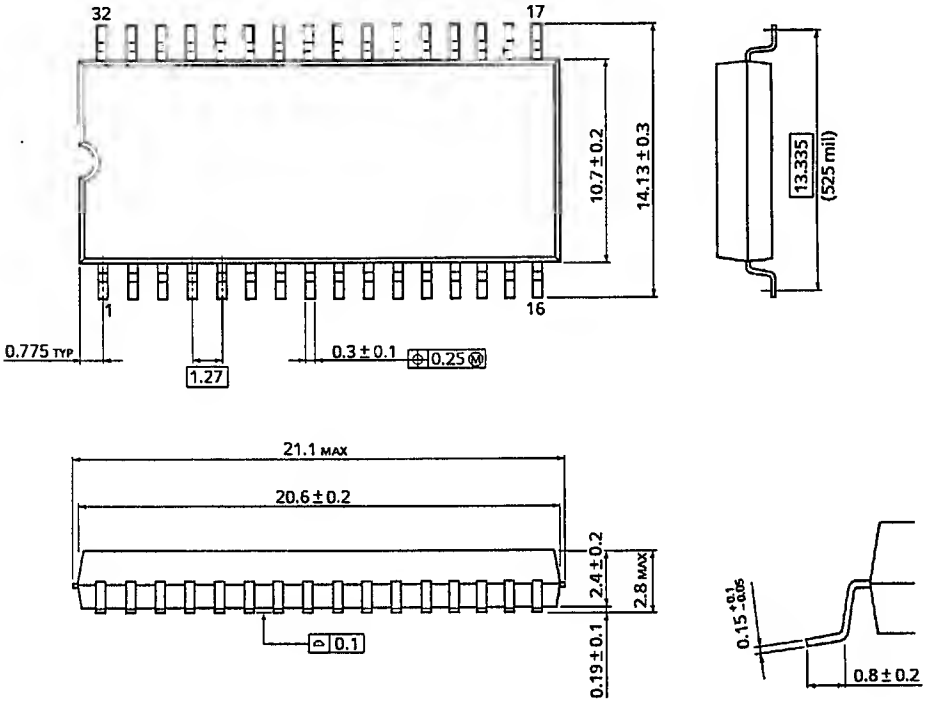
Unit in mm



Weight : 4.53 g (Typ.)

OUTLINE DRAWING (SOP32-P-525)

Unit in mm

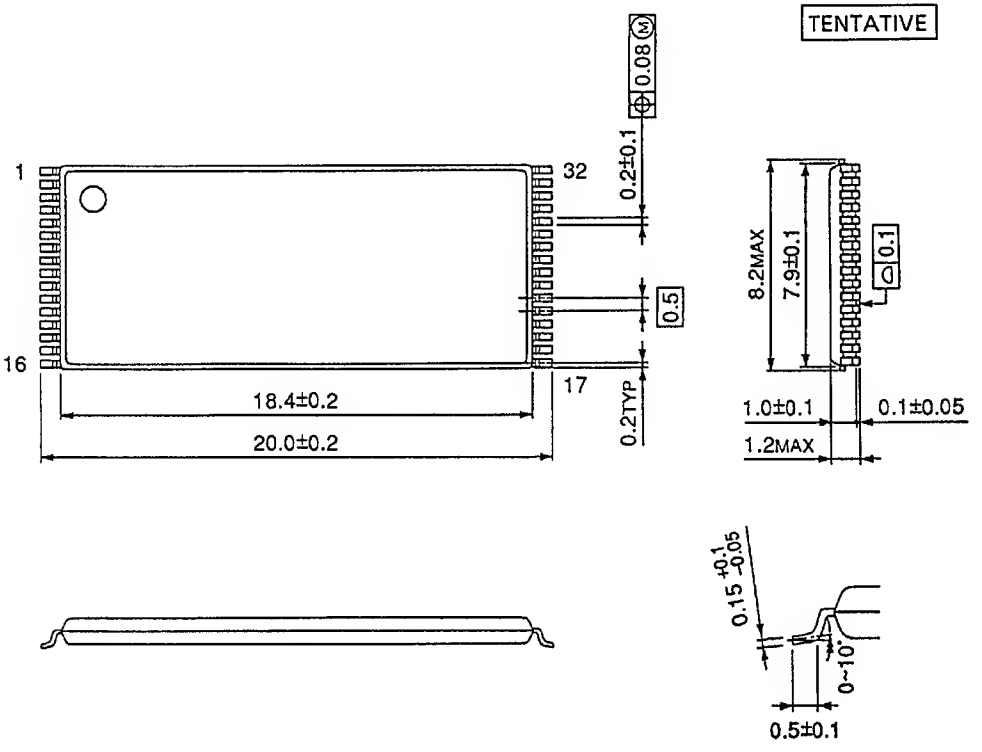


Weight : 1.10 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820)

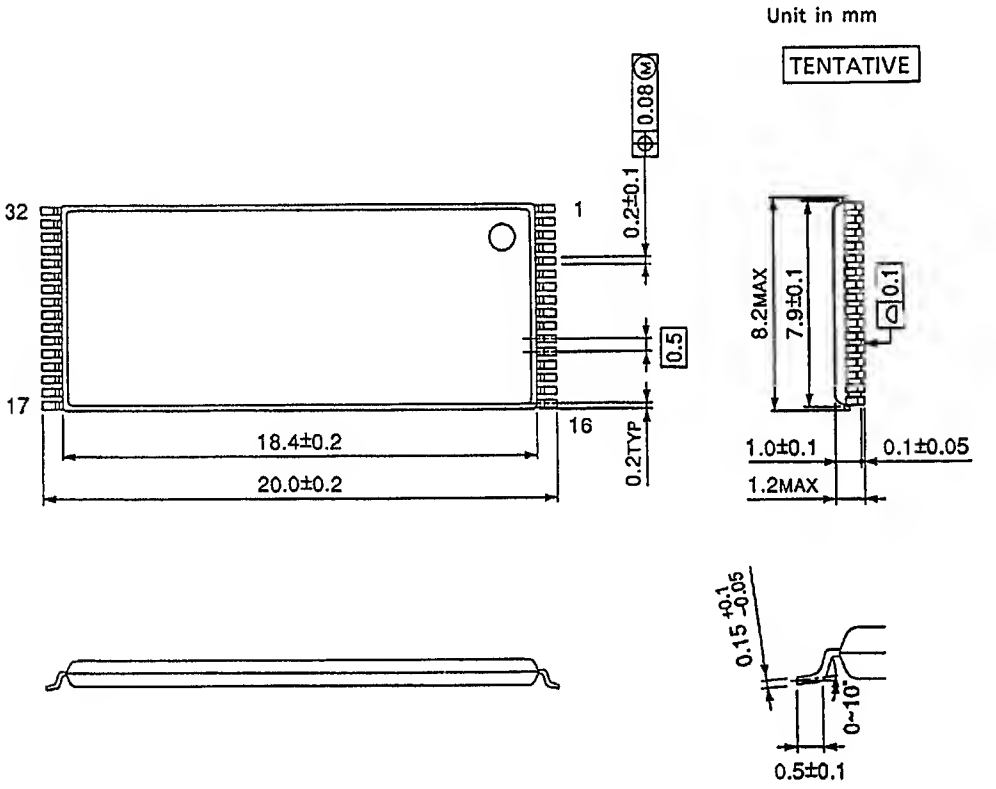
Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820A)



Weight : 0.36 g (Typ.)

131,072 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC551001API is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.)and minimum cycle time of 100ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001API has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001API is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. And TC551001API guarantees −40 ~ 85 °C operating temperature so TC551001API is suitable for use in wide operating temperature system.

The TC551001API is offered in a dual - in - line 32 pin standard plastic package, small - out - line plastic package and thin small - out - line plastic package (forward, reverse type).

FEATURES

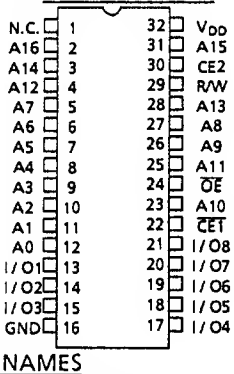
- Low Power Dissipation
  27.5mW / MHz (Typ.) Operating
- Standby Current : 4μA (MAX.) at Ta = 25°C
- 5V Single Power Supply
- Power Down Features : $\overline{CE1}$, CE2
- Data Retention Supply Voltage : 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Wide Temperature Operating : −40~85 °C
- Access Time (MAX.)

Access Time	100ns
$\overline{CE1}$ Access Time	100ns
CE2 Access Time	100ns
$\overline{OE}$ Access Time	50ns

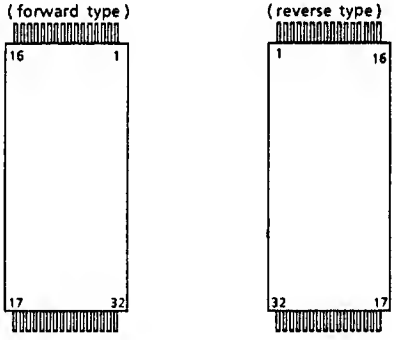
- Package
  TC551001API - L : DIP32-P-600
  TC551001AFI - L : SOP32-P-525
  TC551001AFTI - L : TSOP32-P-0820
  TC551001ATRI - L : TSOP32-P-0820A

PIN CONNECTION (TOP VIEW)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP

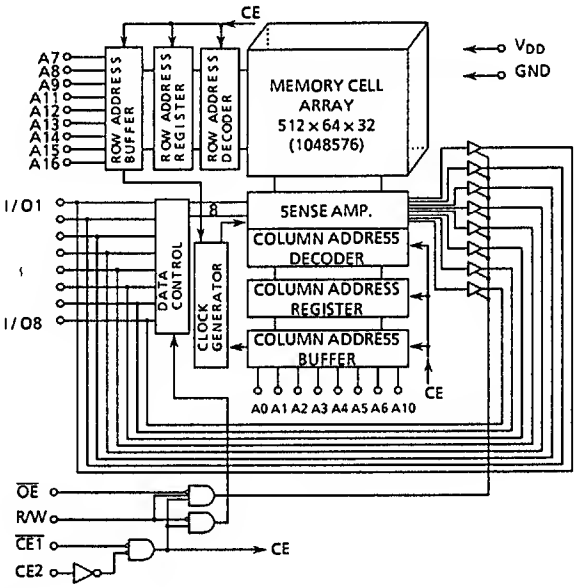


PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+ 5V)
GND	Ground
N.C.	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{OO}	N.C.	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	−40 ~ 85	°C

*: −3.0V at pulse width 50ns MAX. **: SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = -40 ~ 85 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	- 0.3	-	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

D.C. and OPERATING CHARACTERISTICS (Ta = -40 ~ 85 °C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{OD}			-	-	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			-	-	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	Min.	-	-	70	mA
				1 μs	-	-	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD}-0.2V R/W = V_{DD} - 0.2V, I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V / 0.2V	Tcycle	Min.	-	-	60	mA
				1 μs	-	-	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			-	-	3	mA
I_{DDS2} (1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 25°C		-	2	4	μA
			Ta = - 40 ~ 85°C		-	-	70	

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 $\geqq V_{DD}-0.2V$ or CE2 $\leqq$ 0.2V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = -40 ~ 85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	100	-	ns
t_{ACC}	Address Access Time	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	100	
t_{CO2}	CE2 Access Time	-	100	
t_{OE}	Output Enable to Output in Valid	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	40	
t_{ODO}	Output Enable to Output in High-Z	-	40	
t_{OH}	Output Data Hold Time	10	-	

WRITE CYCLE

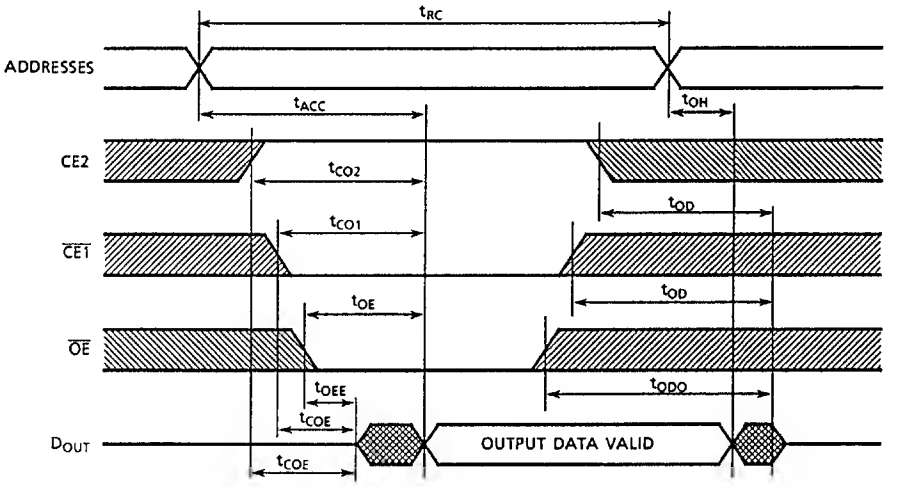
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	100	-	ns
t_{WP}	Write Pulse Width	60	-	
t_{CW}	Chip Selection to End of Write	80	-	
t_{AS}	Address Set up Time	0	-	
t_{WR}	Write Recovery Time	0	-	
t_{ODW}	R/W to Output in High-Z	-	40	
t_{OEW}	R/W to Output in Low-Z	0	-	
t_{DS}	Data Set up Time	40	-	
t_{DH}	Data Hold Time	0	-	

A.C. TEST CONDITIONS

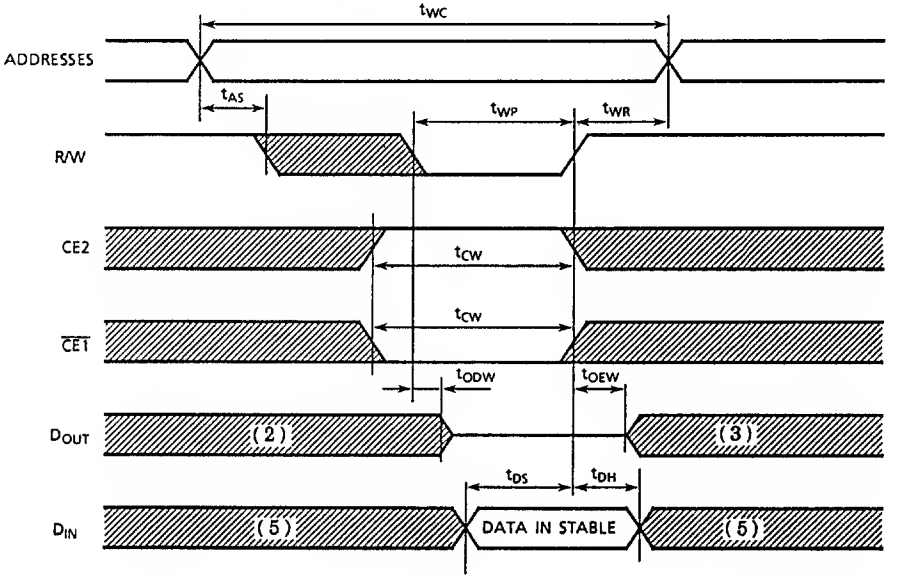
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.4V, 2.6V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

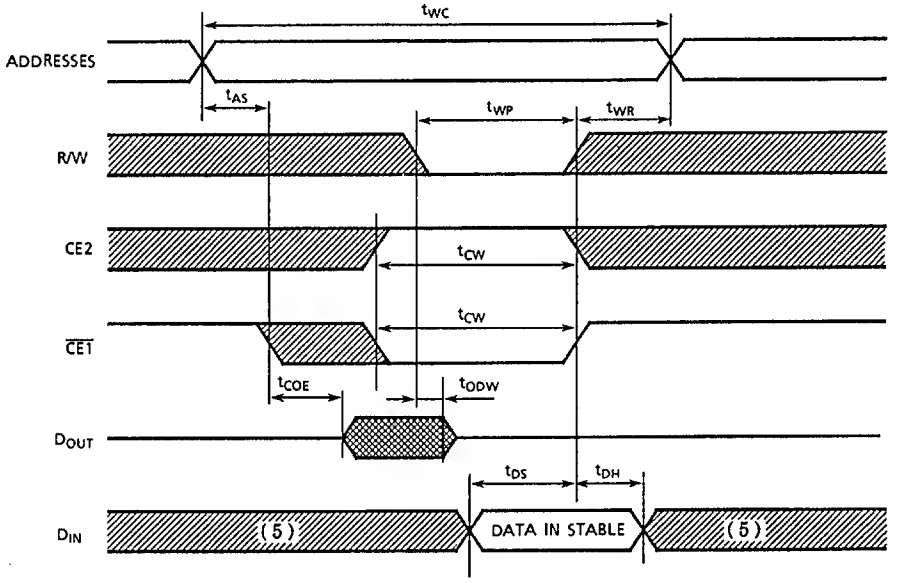
READ CYCLE (1)



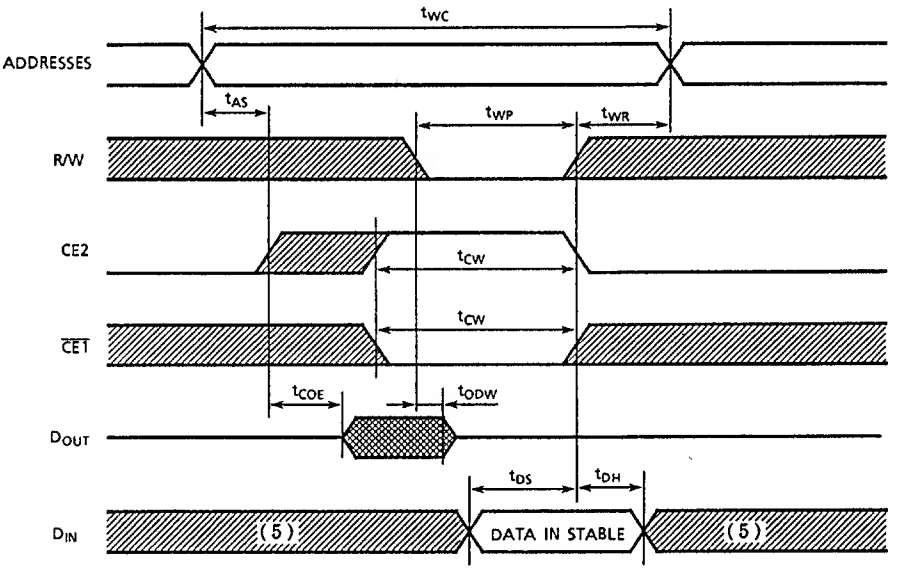
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

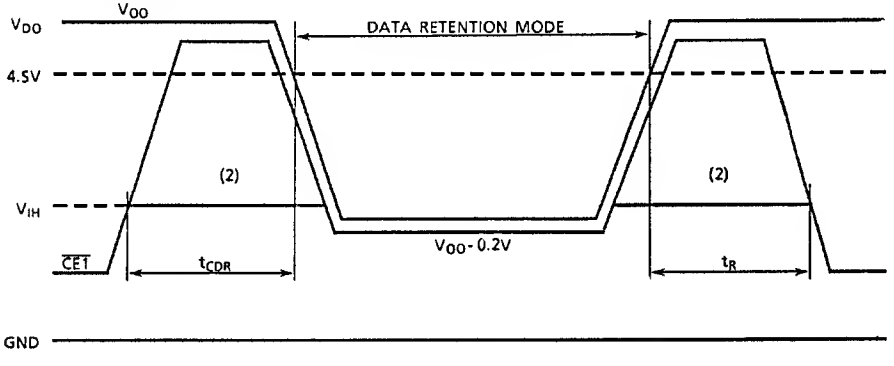
(5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = −40 ~ 85 °C)

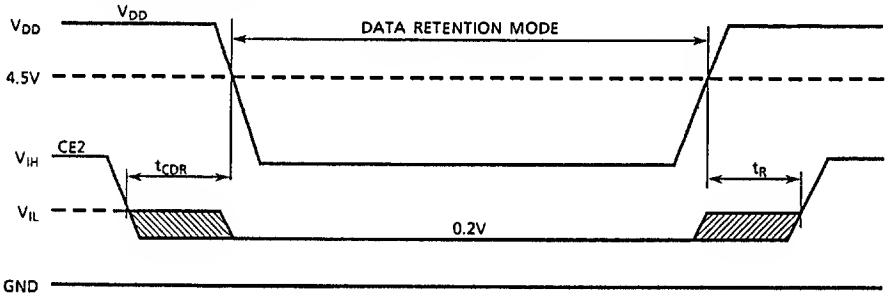
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{OH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{OOS2}	Standby Current	V_{DD} = 3.0V	-	-	35*	μA
		V_{OO} = 5.5V	-	-	70	
t_{COR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

*) 3μA (MAX.) Ta = −40 ~ 40 °C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

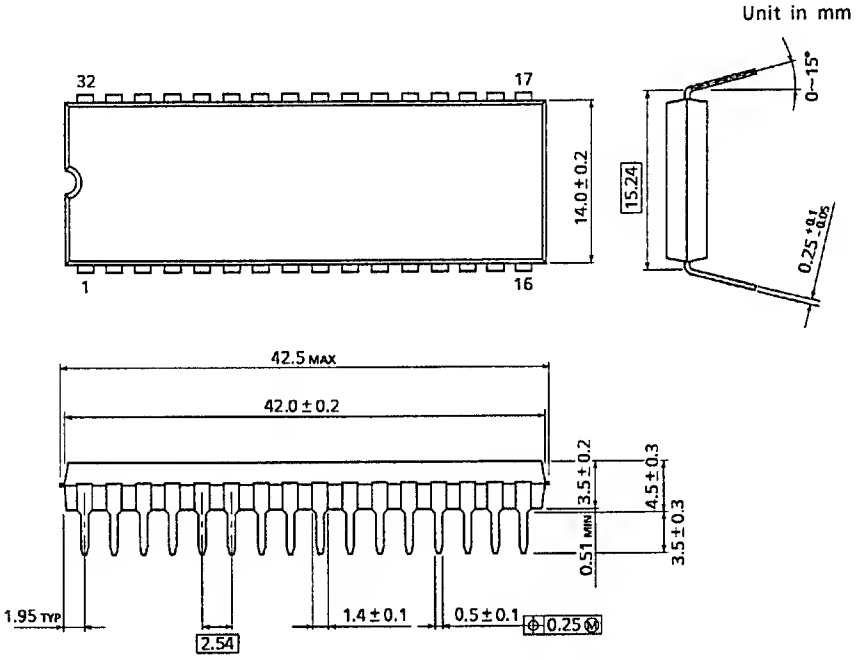
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32-P-600)

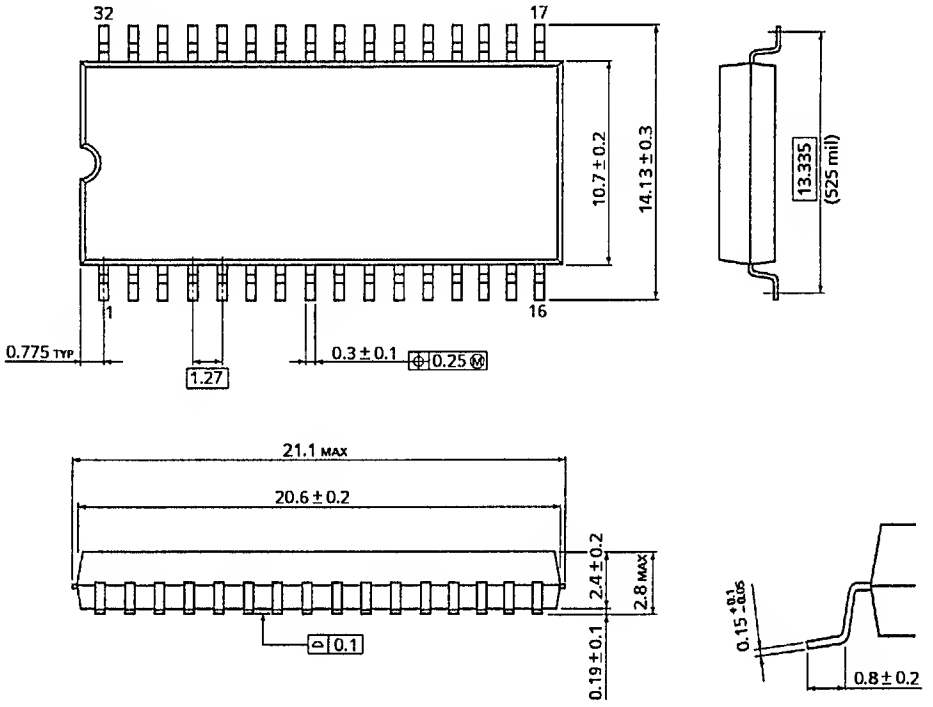
Unit in mm



Weight : 4.53 g (Typ.)

OUTLINE DRAWING (SOP32-P-525)

Unit in mm

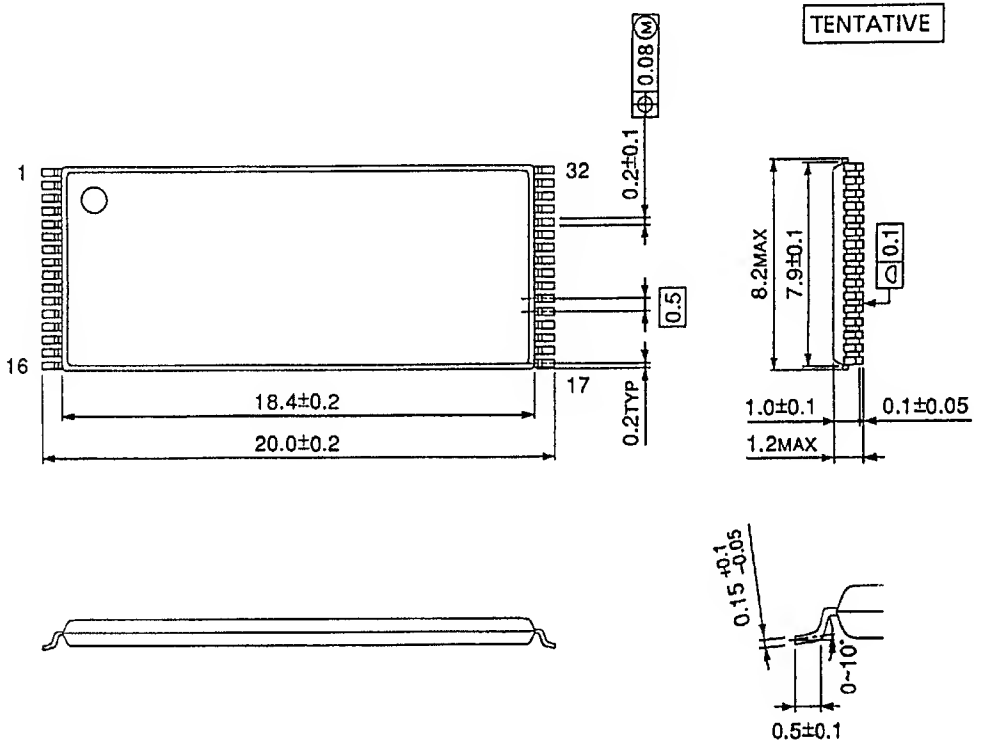


Weight : 1.10 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820)

Unit in mm

TENTATIVE

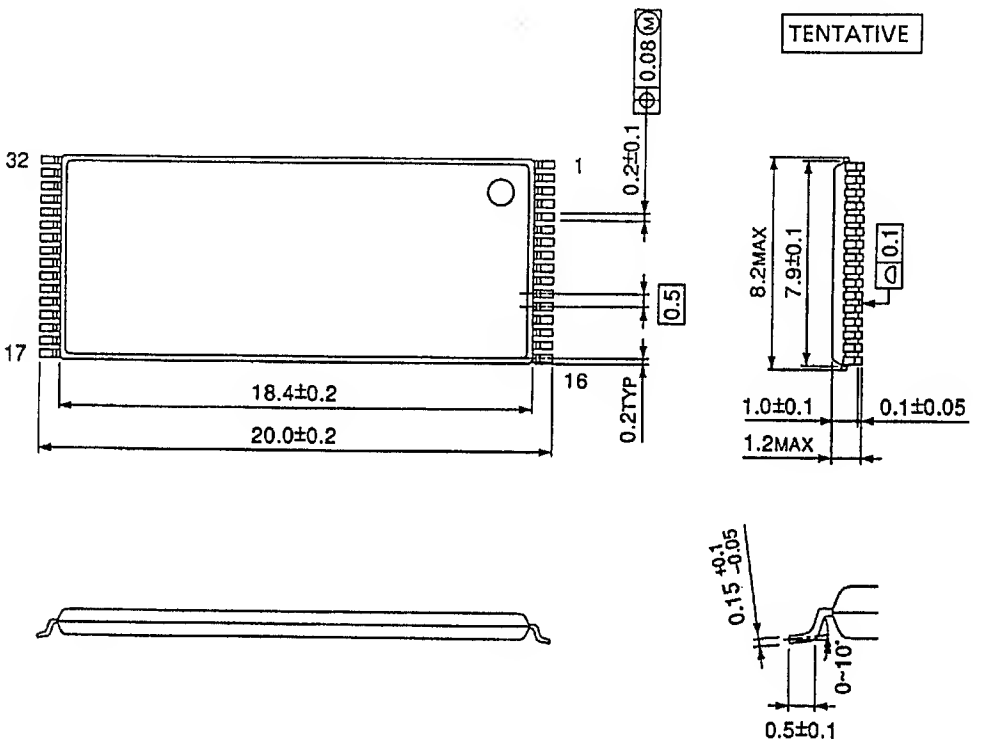


Weight : 0.36 g (Typ.)

OUTLINE DRAWING (TSOP32-P-0820A)

Unit in mm

TENTATIVE



Weight : 0.36 g (Typ.)

CMOS High Speed Static RAM

8,192 WORD × 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5588P/J is a 65,536 bits high speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit from provides high speed feature.

The TC5588P/J has low power feature with device control using Chip Enable ($\overline{CE1}$/CE2), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

The TC5588P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC5588P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time:

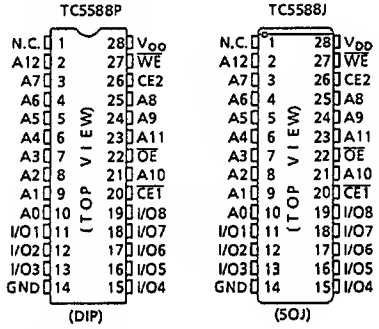
TC5588P/J-15	15ns (MAX.)
TC5588P/J-20	20ns (MAX.)
TC5588P/J-25	25ns (MAX.)
TC5588P/J-35	35ns (MAX.)

- Low power dissipation:

Operation	TC5588P/J-15	135mA (MAX.)
	TC5588P/J-20	115mA (MAX.)
	TC5588P/J-25	115mA (MAX.)
	TC5588P/J-35	115mA (MAX.)
Standby		1mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : $\overline{OE}$
- Package
  - TC5588P : DIP28-P-300B
  - TC5588J : SOJ28-P-300A

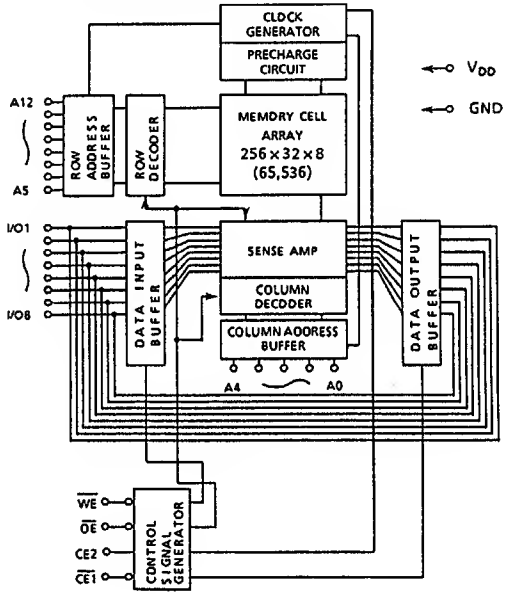
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	*-3.0	-	0.8	V

* Pulse width ≦ 10ns, DC : −0.5V (min)

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		-	-	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}		-	-	±1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL} I_{OUT} = 0mA	-15	-	-	135	mA
			-20				
			-25	-	-	115	
			-35				
I_{DDS1}	Standby Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}		-	-	25	mA
I_{DDS2}*		$\overline{CE1}$ = V_{DD}-0.2V or CE2 = 0.2V Other Inputs = V_{DD}-0.2V or 0.2V		-	-	1	

*: In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $\overline{CE2} \geqq V_{DD}-0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO1}	$\overline{CE1}$ Access Time	–	15	–	20	–	25	–	35	
t_{CO2}	CE2 Access Time	–	15	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	12	
t_{OH}	Output Data Hold Time From Address Change	5	–	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	6	–	6	–	6	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	
t_{OOD}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	15	–	20	–	25	–	35	

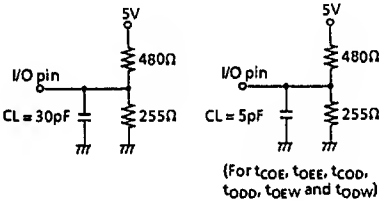
WRITE CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	15	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	
t_{WP}	Write Pulse Width	12	–	13	–	15	–	15	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	9	–	10	–	12	–	12	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	

AC TEST CONDITIONS

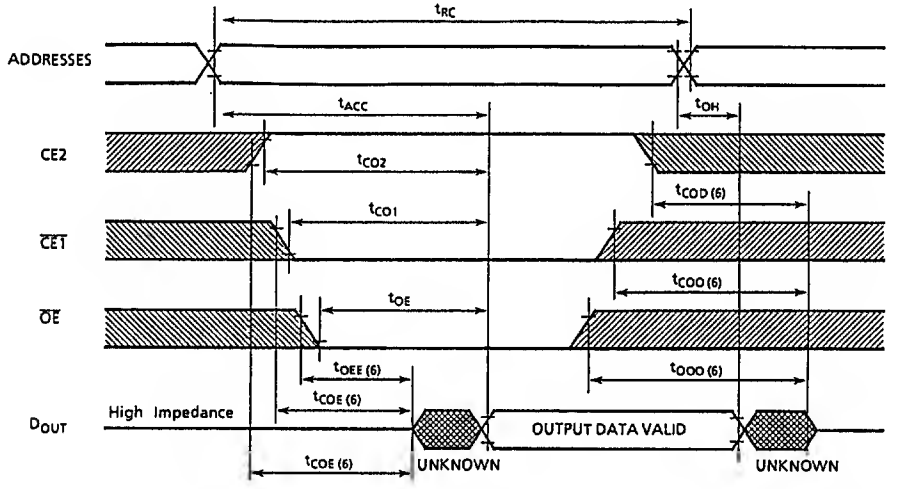
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

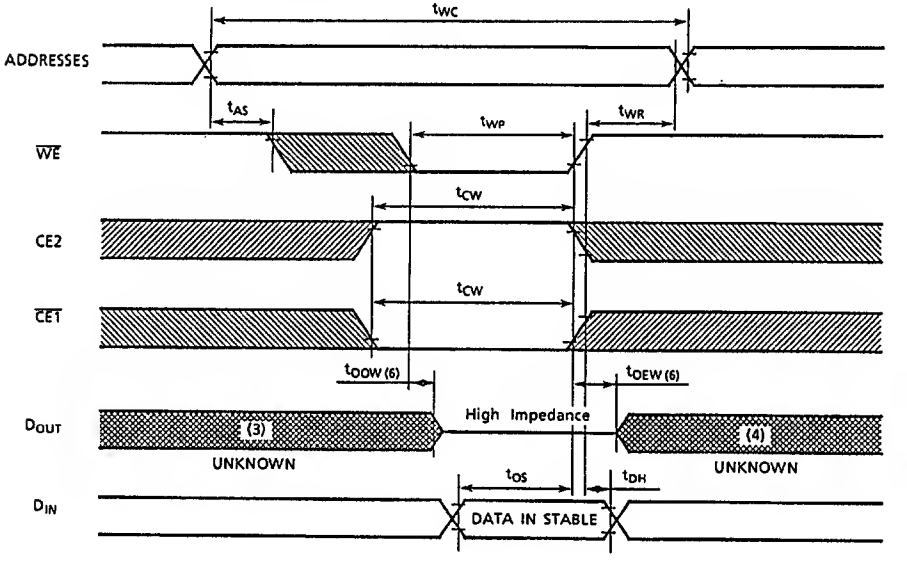


TIMING WAVEFORMS

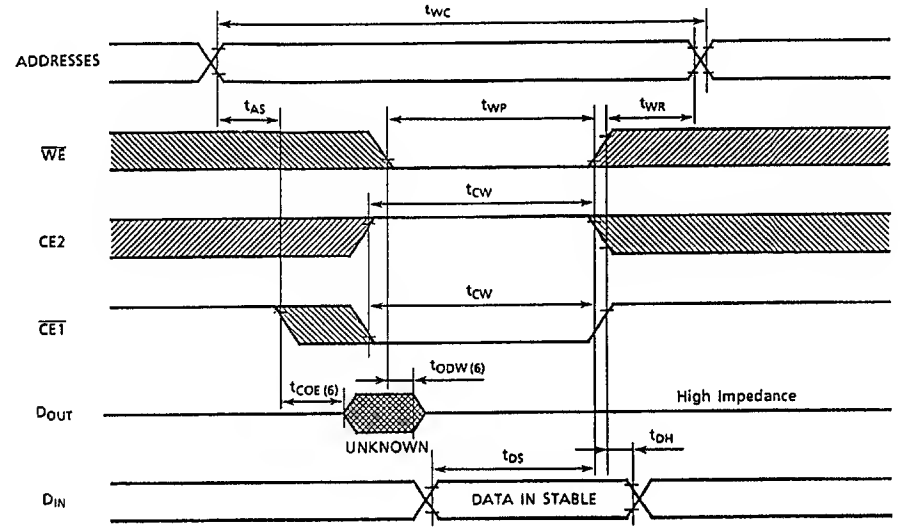
READ CYCLE (2)



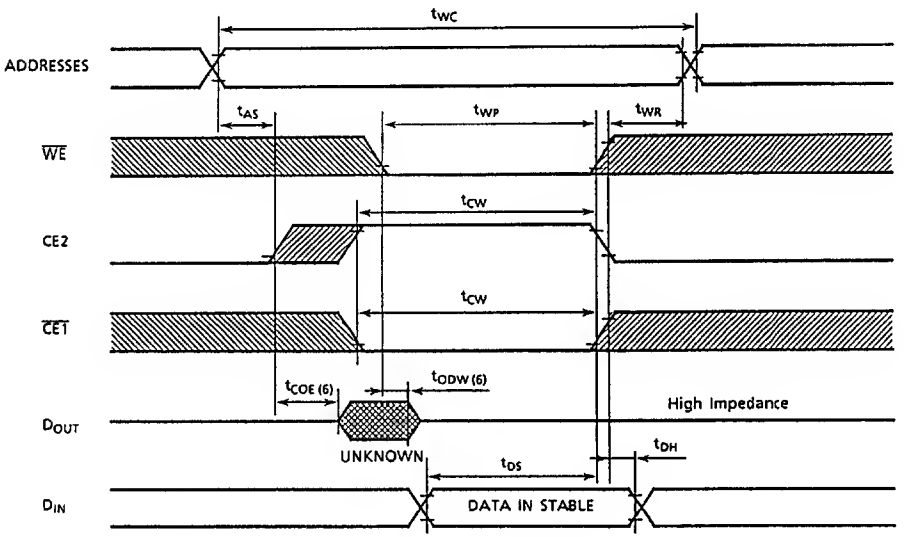
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYLCE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High t ransition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

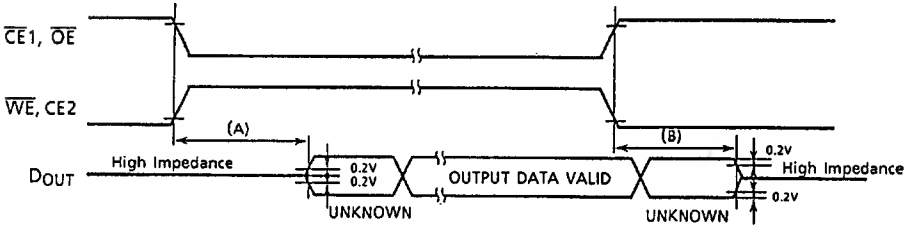
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

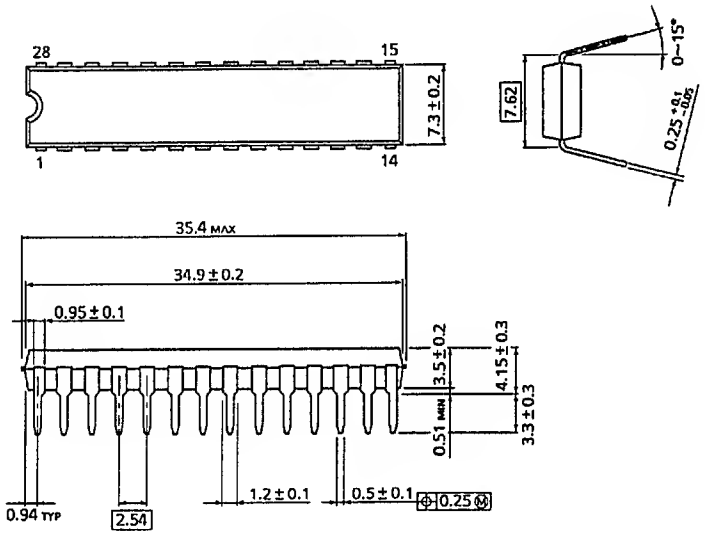
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28−P−300B)

UNIT in mm

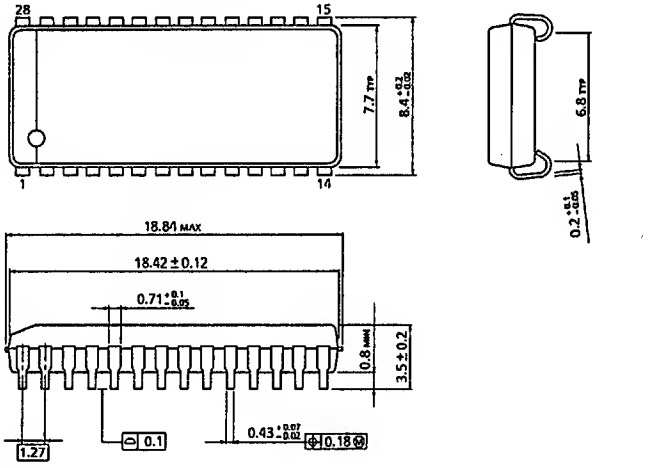


Weight : 2.03 g (TYP)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28−P−300A)

UNIT in mm



Weight : 0.83 g (TYP)

8,192 WORD×9 BIT CMOS STATIC RAM

DESCRIPTION

The TC5589P/J is a 73,728 bits high speed static random access memory organized as 8,192 words by 9 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit from provides high speed feature.

The TC5589P/J has low power feature with device control using Chip Enable ($\overline{CE1}$/CE2), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

The TC5589P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC5589P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time:

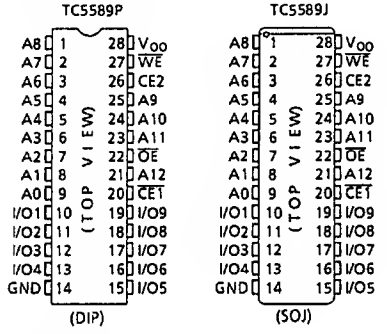
	TC5589P/J-15	15ns (MAX.)
	TC5589P/J-20	20ns (MAX.)
	TC5589P/J-25	25ns (MAX.)
	TC5589P/J-35	35ns (MAX.)

- Low power dissipation:

Operation	TC5589P/J-15	135mA (MAX.)
	TC5589P/J-20	115mA (MAX.)
	TC5589P/J-25	115mA (MAX.)
	TC5589P/J-35	115mA (MAX.)
Standby		1mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : $\overline{OE}$
- Package
  - TC5589P : DIP28-P-300B
  - TC5589J : SOJ28-P-300A

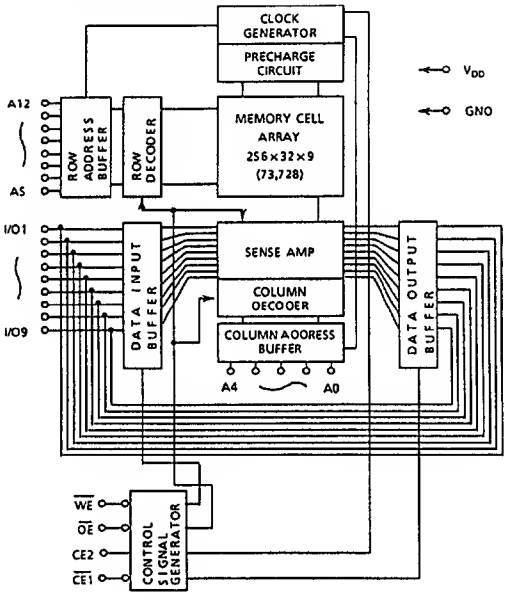
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	*−3.0	−	0.8	V

* Pulse width ≦ 10ns, DC: −0.5V (min)

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}		−	−	±1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL} I_{OUT} = 0mA	−15	−	−	135	mA
			−20				
			−25	−	−	115	
			−35				
I_{DDS1}	Standby Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}		−	−	25	mA
I_{DDS2}*		$\overline{CE1}$ = V_{DD} − 0.2V or CE2 = 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V		−	−	1	

* : In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD}-0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO1}	$\overline{CE1}$ Access Time	–	15	–	20	–	25	–	35	
t_{CO2}	CE2 Access Time	–	15	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	12	
t_{OH}	Output Data Hold Time From Address Change	5	–	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	6	–	6	–	6	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	15	–	20	–	25	–	35	

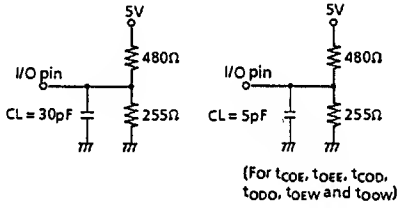
WRITE CYCLE

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	15	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	
t_{WP}	Write Pulse Width	12	–	13	–	15	–	15	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	9	–	10	–	12	–	12	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

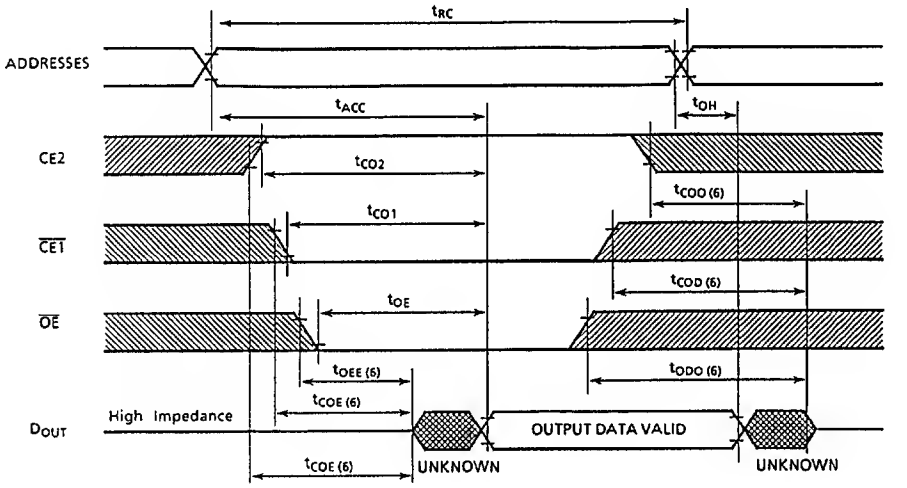
Fig. 1



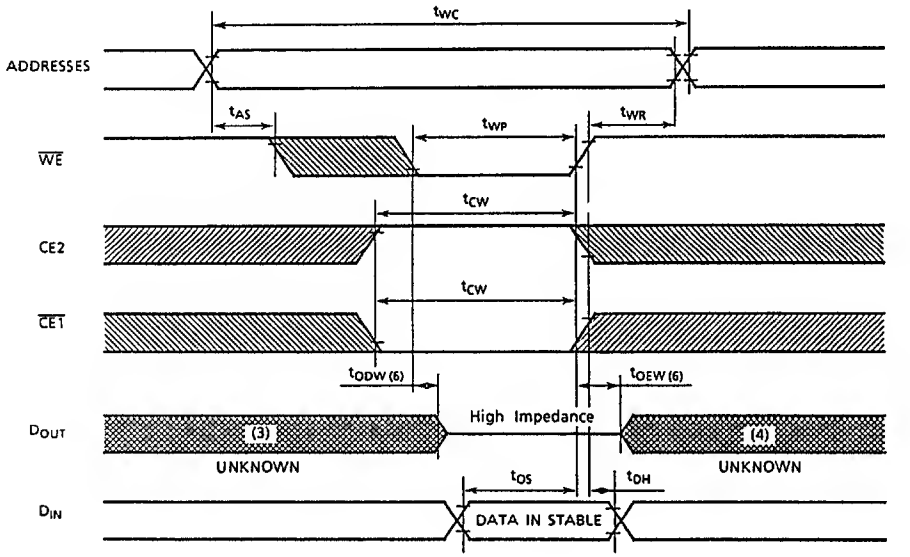
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{OOW})

TIMING WAVEFORMS

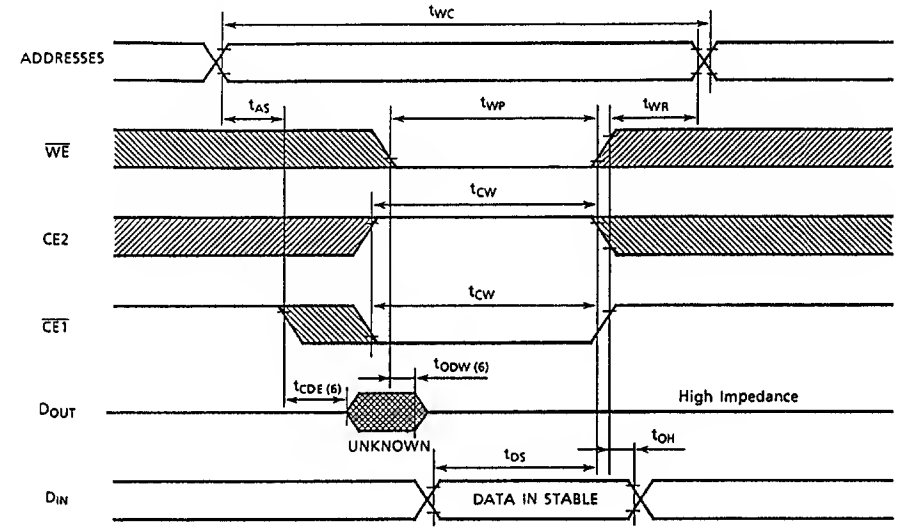
READ CYCLE (2)



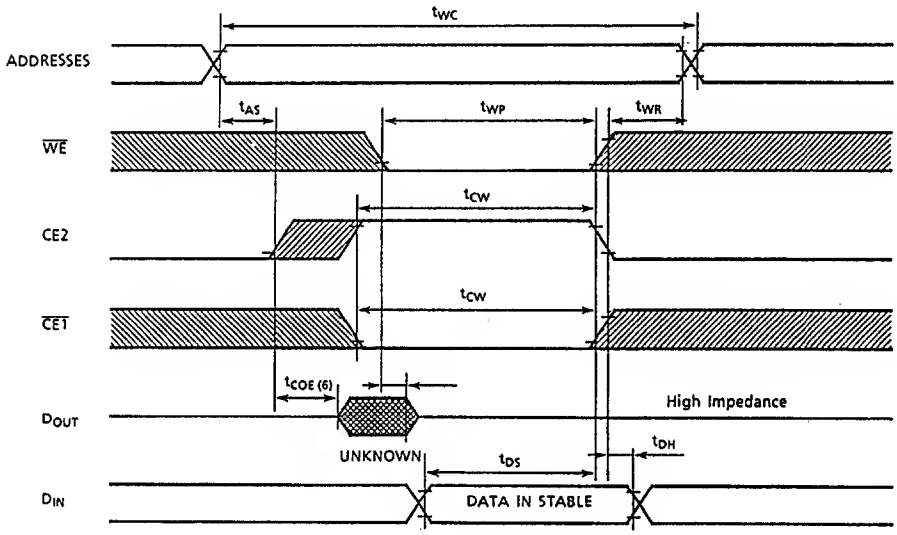
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYLCE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High t ransition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

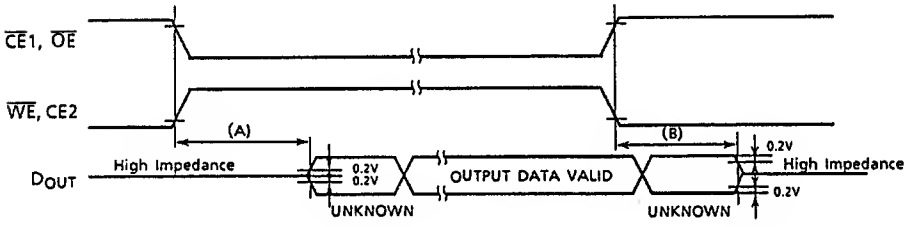
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

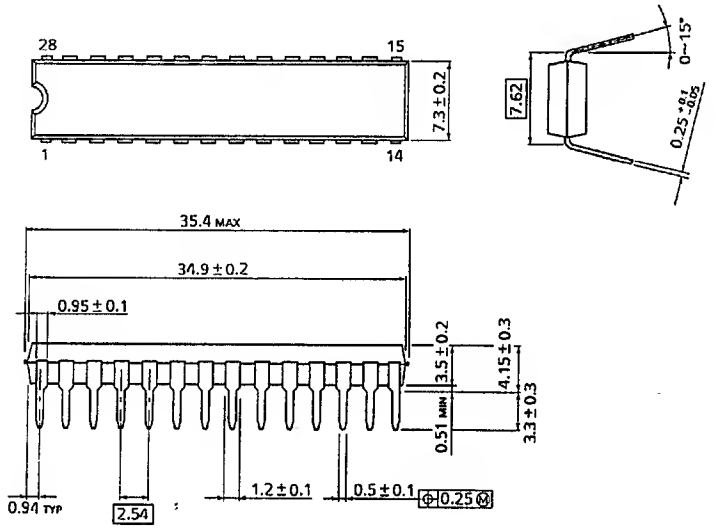
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28−P−300B)

UNIT in mm

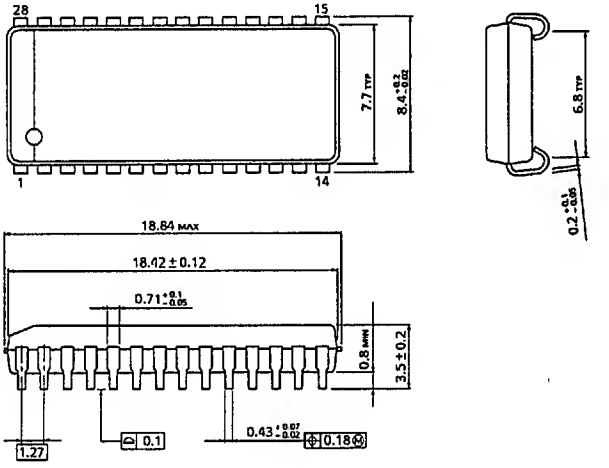


Weight : 2.03 g (TYP)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28−P−300A)

UNIT in mm



Weight : 0.83 g (TYP)

16,384 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55416P-H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 15ns / 20ns / 25ns / 35ns and maximum operating current of 120mA / 100mA / 100mA / 80mA at minimum cycle time.

The TC55416P-H also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA.

The TC55416P is suitable for use in cache memory and high speed storage, where high speed / high density are required.

The TC55416P-H is packaged in a 22 pin standard plastic DIP with 0.3 inch width for high density assembly.

The TC55416P-H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time :

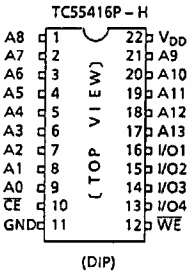
TC55416P-15H	15ns(MAX.)
TC55416P-20H	20ns(MAX.)
TC55416P-25H	25ns(MAX.)
TC55416P-35H	35ns(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Diractly TTL compatible :
  All Input and Output
- Low power dissipation :

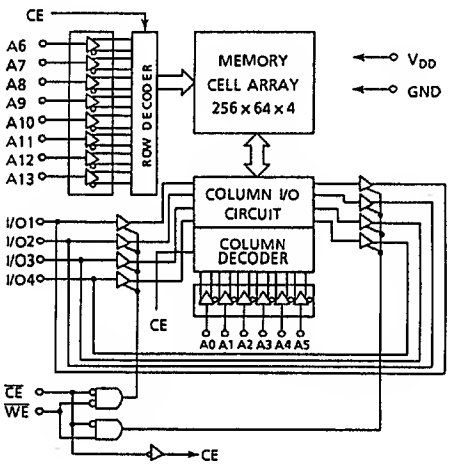
Operation	TC55416P-15H	120mA(MAX.)
	TC55416P-20H	100mA(MAX.)
	TC55416P-25H	100mA(MAX.)
	TC55416P-35H	80mA(MAX.)
Standby		1mA(MAX.)

- Package
  TC55416P-H : DIP22-P-300

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{DO}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Output Voltage	-0.5~V_{DO}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
T_{strg}	Strage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
V_{DO}	Poser Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{OO}+0.5	V
V_{IL}	Input Low Voltage	*-3.0	-	0.8	V

* Pulse width ≦10ns, DC : -0.5V (min)

DC and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	CHARACTERISTIC	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{OO}		-	-	±1	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=0~V_{DO}		-	-	±1	μA
I_{OOO}	Operating Current	V_{DO}=5.5V, tcycle=Min cycle $\overline{CE}$=V_{IL}, I_{OUT}=0mA Other Input=V_{IH}/V_{IL}	-15H	-	-	120	mA
			-20H	-	-	100	
			-25H	-	-	100	
			-35H	-	-	80	
I_{DDS1}	Standby Current	V_{DO}=5.5V, tcycle=Min cycle $\overline{CE}$=V_{IH}, Other Input=V_{IH}/V_{IL}		-	-	25	mA
I_{OOS2}		$\overline{CE}$=V_{OO}-0.2V Other Input=V_{DO}-0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta=25°C)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

AC CHARACTEIRSTICS ($Ta=0\sim70°C$ [4], $V_{DD}=5V\pm10\%$)

READ CYCLE

SYMBOL	CHARACTERISTIC	TC55416P-15H		TC55416P-20H		TC55416P-25H		TC55416P-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	15	-	20	-	25	-	35	
t_{CO}	Chip Enable Access Time	-	15	-	20	-	25	-	35	
t_{COE}	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	6	-	6	-	6	-	6	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	5	-	
t_{PU}	Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Power Down Time	-	15	-	20	-	25	-	35	

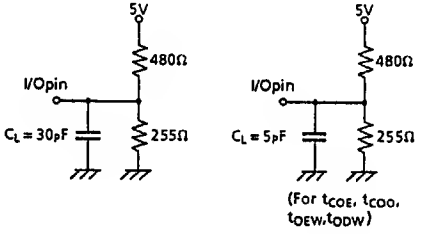
WRITE CYCLE

SYMBOL	CHARACTERISTIC	TC55416P-15H		TC55416P-20H		TC55416P-25H		TC55416P-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t_{WP}	Write Pulse Width	12	-	13	-	13	-	13	-	
t_{CW}	Chip Enable to End of Write	12	-	13	-	13	-	13	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	6	-	6	-	6	-	6	
t_{DS}	Data Set Up Time	9	-	10	-	10	-	10	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0	-	

AC TEST CONDITIONS

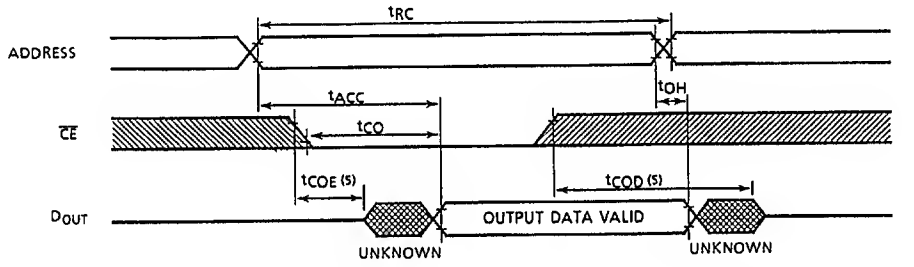
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

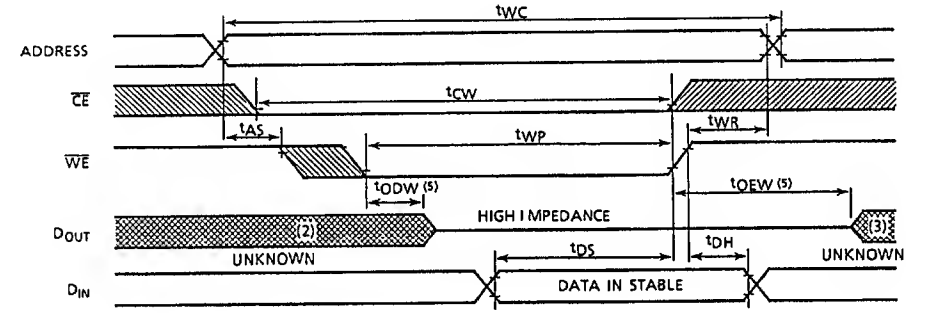


TIMING WAVEFORMS

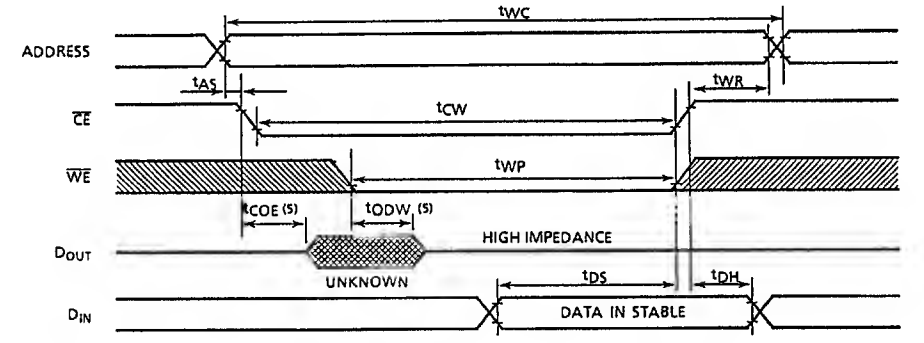
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



(注) 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

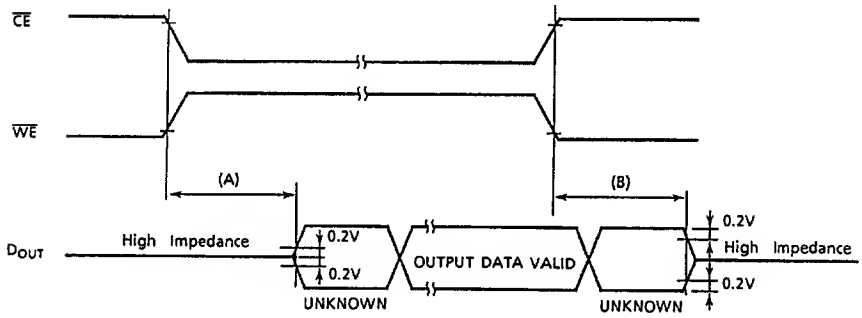
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEW} ····· Output Enable Time

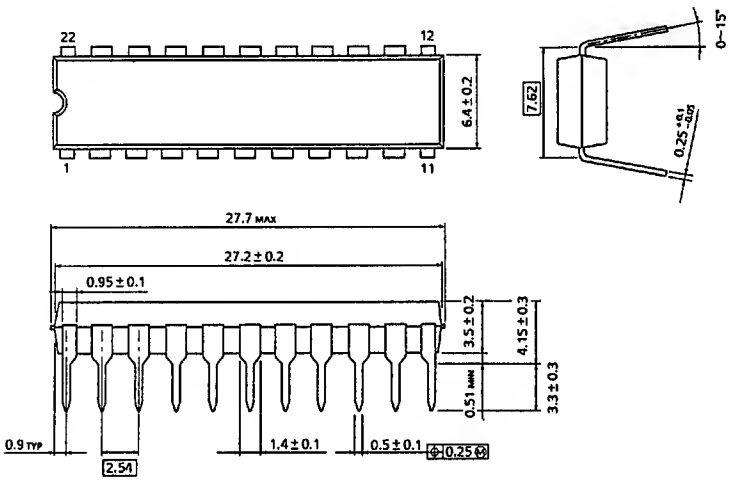
   (B) t_{COD}, t_{ODW} ····· Output Disable Time



OUTPUT DRAWINGS

Plastic DIP (DIP22−P−300)

UNIT in mm



WEIGHT : 1.44g (Typ.)

16,384 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55417P/J-H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5 - volt supply. Toshiba's high performance device technolgy provides both high speed and low power features with a maximum access time of 15ns / 20ns / 25ns / 35ns and maximum operating current of 120mA / 100mA / 100mA / 80mA at minimum cycle time.

The TC55417P/J-H also features an automatic stand - by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA.

The TC55417P/J-H is suitable for use in cache memory and high speed storage, where high speed / high density are required.

The TC55417P/J-H is packaged in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

The TC55417P/J-H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time :

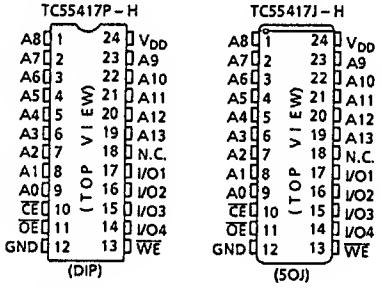
	TC55417P/J-15H	15ns(MAX.)
	TC55417P/J-20H	20ns(MAX.)
	TC55417P/J-25H	25ns(MAX.)
	TC55417P/J-35H	35ns(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Diractly TTL compatible :
  All Input and Output
- Low power dissipation :

Operation	TC55417P/J-15H	120mA(MAX.)
	TC55417P/J-20H	100mA(MAX.)
	TC55417P/J-25H	100mA(MAX.)
	TC55417P/J-35H	80mA(MAX.)
Standby		1mA(MAX.)

- Outpot buffer control : $\overline{OE}$
- Package
  TC55417P-H : DIP24-P-300B
  TC55417J-H : SOJ24-P-300A

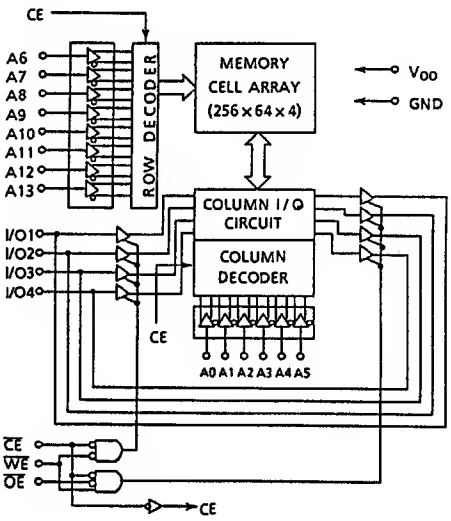
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+ 5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{OO}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	$-0.5 \sim V_{DD}+0.5$	V
P_D	Power Dissipation	650	mW
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{OD}+0.5$	V
V_{IL}	Input Low Voltage	*-3.0	-	0.8	V

* Pulse width ≦10ns, DC : −0.5V (min)

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-4	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0 \sim V_{OD}$		-	-	±1	μA
I_{OOO}	Operating Current	$V_{DD}=5.5V$, tcycle = Min cycle $\overline{CE}=V_{IL}$, $I_{OUT}=0mA$ Other Input = V_{IH}/V_{IL}	-15H	-	-	120	mA
			-20H	-	-	100	
			-25H	-	-	100	
			-35H	-	-	80	
I_{OOS1}	Standby Current	$V_{DD}=5.5V$, tcycle = Min cycle $\overline{CE}=V_{IH}$, Other Input = V_{IH}/V_{IL}		-	-	25	mA
I_{DDS2}		$\overline{CE}=V_{OO}-0.2V$ Other Input = $V_{DD}-0.2V$ or 0.2V		-	-	1	

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

Note : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ [4], $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	ns
t_{CO}	Chip Enable Access Time	–	15	–	20	–	25	–	35	ns
t_{OE}	Output Enable to Output Valid	–	9	–	10	–	10	–	10	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	6	–	6	–	6	–	6	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	ns
t_{OH}	Output Data Hold Time	5	–	5	–	5	–	5	–	ns
t_{PU}	Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PO}	Power Down Time	–	15	–	20	–	25	–	35	ns

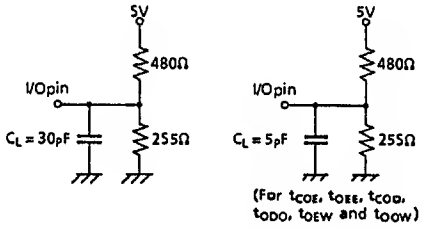
WRITE CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	13	–	13	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	13	–	13	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	ns
t_{OS}	Data Set Up Time	9	–	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns

AC TEST CONDITIONS

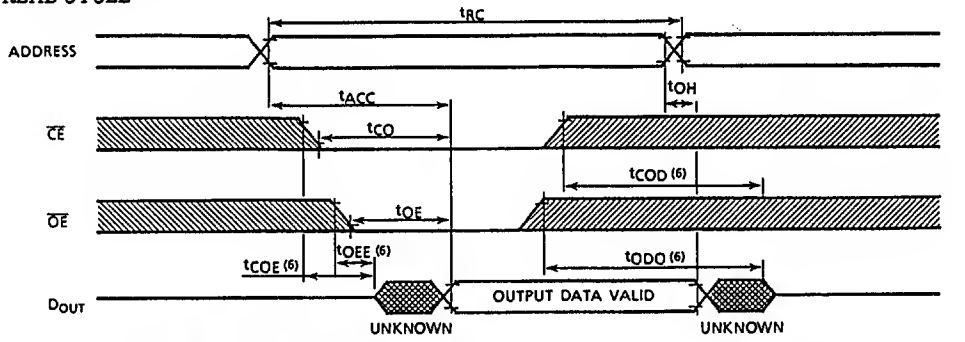
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

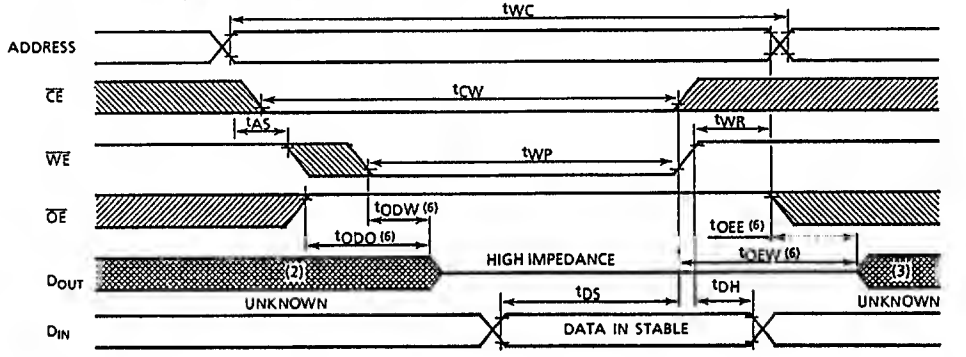


TIMING WAVEFORMS

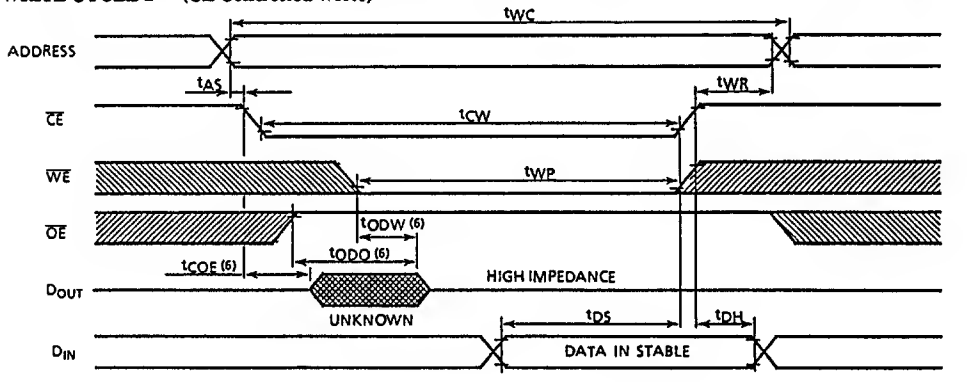
READ CYCLE [1]



WRITE CYCLE 1 [5] ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 [6] ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occures coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

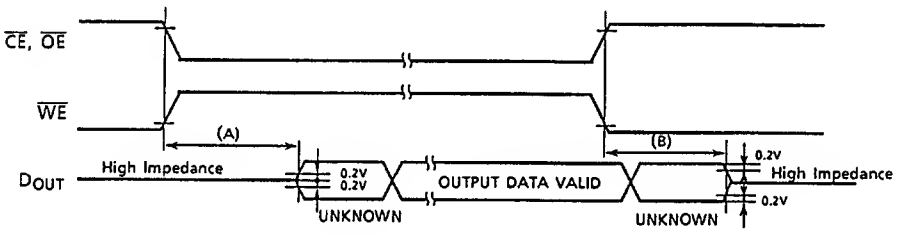
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

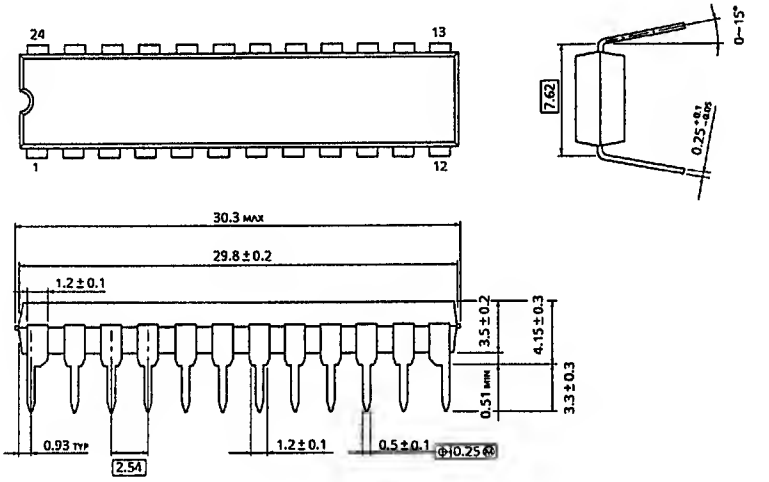
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP−24−300B)

Unit in mm

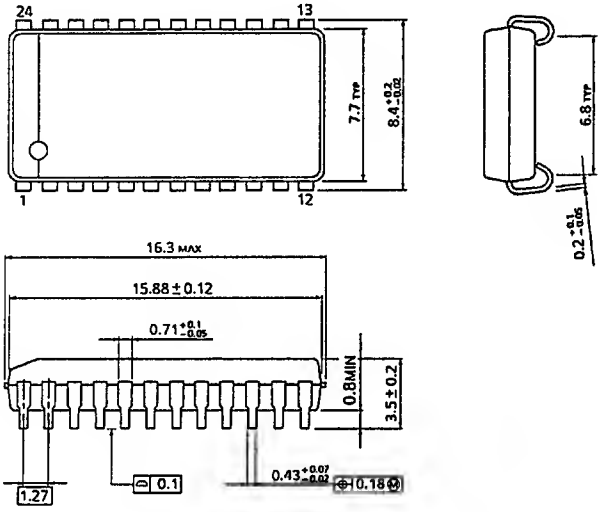


Weight : 1.72 g (TYP)

OUTLINE DRAWINGS

Plastic SOJ (SOJ24−P−300A)

Unit in mm



Weight : 0.72 g (TYP)

2-WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS
CMOS STATIC CACHE DATA RAM

DESCRIPTION

The TC55187T is a 147,456 bits high-speed static RAM which can be user-configured either as 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with a byte control and on-chip address latches. The TC55187T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed feature, and is operated from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolar TTL circuits. The TC55187T can directly interface with the INTEL 82385 cache controller, without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore; Significant reductions in the number of parts, board assembly area and power dissipation can be achieved by using the TC55187T cache data RAM. The MODE input of the TC55187T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bits organization which is suitable for 2-way set associative cache designs or as a 8,192 words by 18 bits organization suitable for direct map cache designs. The TC55187T can also be operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55187T is packaged in a 52-pin standard PLCC for high-density board level assembly.

FEATURES

- Fast Access Time (max.)

ITEM		TC55187T		
		-20	-25	-30
t_{RC}	Cycle Time	20ns	25ns	30ns
t_{AA}	Address Access Time	20ns	25ns	30ns
t_{OE}	$\overline{OE}$ Access Time	10ns	10ns	12ns

- Power dissipation

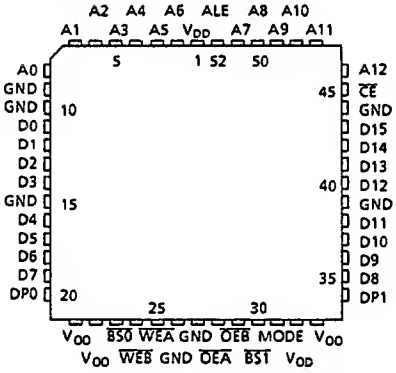
Operating	TC55187T-20	230mA (max.)
	TC55187T-25	220mA (max.)
	TC55187T-30	200mA (max.)
Standby		40mA (max.)

- Configurable for 2-way or direct RAM arrays
  2-way 4,096words×18bits (MODE = V_{IH})
  8,192words×18bits (MODE = V_{IL})
- Contains address latches (except A12) and byte control, $\overline{BS0}$ and $\overline{BS1}$
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : $\overline{OEA}$, $\overline{OEB}$
- Two Write enable controls : $\overline{WEA}$, $\overline{WEB}$
- TC55187T: QFJ52-P-S750

PIN NAMES

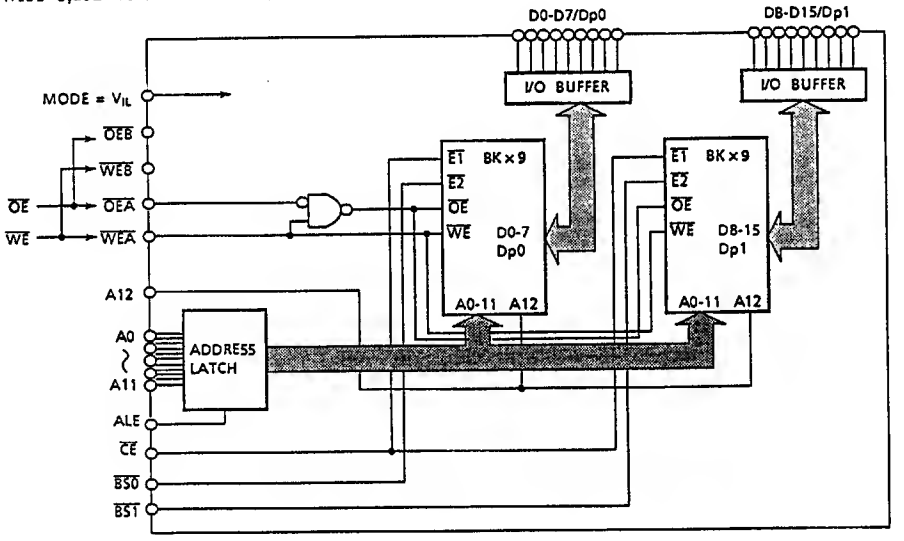
A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input/Output
ALE	Address Latch Input
$\overline{CE}$	Chip Enable Input
$\overline{BS0}$	Lower Byte Select Input
$\overline{BS1}$	Upper Byte Select Input
$\overline{OEA}$	Output Enable Input (Way-A)
$\overline{OEB}$	Output Enable Input (Way-B)
$\overline{WEA}$	Write Enable Input (Way-A)
$\overline{WEB}$	Write Enable Input (Way-B)
MODE	Mode Select Input
VDD	Power (+5V)
GND	Ground

PIN CONNECTION (TOP VIEW)

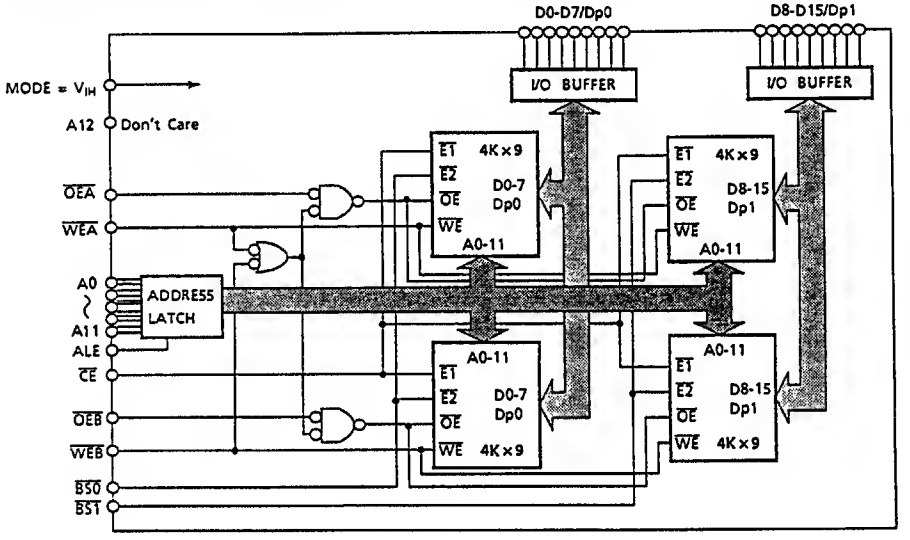


BLOCK DIAGRAM

1−WAY 8,192 words × 18 bits (MODE : V_{IL})



2−WAY 4,096 words × 18 bits (MODE : V_{IH})



TRUTH TABLE 1

CONTROL INPUT			FUNCTION			CONFIGURATION
MODE	ALE	$\overline{CE}$	CHIP	A0~A11	A12	
H	*1	H	Disable	*2	*2	4K × 18 × 2
H	H	L	Enable	Valid	*2	
H	L	L	Enable	Latched	*2	
L	*1	H	Disable	*2	*2	8K × 18
L	H	L	Enable	Valid	Valid	
L	L	L	Enable	Latched	Valid	

*1 : H or L *2 : Don't Care

TRUTH TABLE 2 (MODE = V_{IL} ··· 8K × 18)

INPUTS						OPERATION		
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	CHIP	D0-D7 Dp0	D8-D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	H	L	H	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	L	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			
L	H	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			

* : H or L

TRUTH TABLE 3 (MODE = V_{IH} ··· 4K x 18 x 2)

INPUTS						OPERATION			
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	way-A	way-B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way-B Output	Open
				H	L			Open	way-B Output
				L	L			way-B Output	way-B Output
H	H	L	H	L	H	Read Cycle	Deselect	way-A Output	Open
				H	L			Open	way-A Output
				L	L			way-A Output	way-A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way-B Input	Open
				H	L			Open	way-B Input
				L	L			way-B Input	way-B Input
L	H	*	*	L	H	Write Cycle	Deselect	way-A Input	Open
				H	L			Open	way-A Input
				L	L			way-A Input	way-A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way-A/B Input	Open
				H	L			Open	way-A/B Input
				L	L			way-A/B Input	way-A/B Input

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.3	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C) (1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5*	−	0.8	V

* : −3V pulse width less than 10ns

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−1	−	+1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	Output Disable		−1	−	+1	μA
I_{DDO}	Operating Current	t_{RC}, t_{WC} = min. cycle Add., $\overline{WE}$, ALE = Clock (3.0V/0V) $\overline{OE}$ = 3.0V $\overline{CE}$, $\overline{BS}$ = 0V, MODE = 3.0V / 0V	−20	−	−	230	mA
			−25	−	−	220	
			−30	−	−	200	
I_{DDS}	Standby Current	$\overline{CE}$, $\overline{BS}$, $\overline{WE}$, $\overline{OE}$ = V_{IH}, ALE = V_{IL} Add., Data, MODE = V_{IH} or V_{IL}		−	−	40	mA

CAPACITANCE (Ta = 25°C, freq. = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cin	Input Capacitance	V_{IN} = GND	−	−	5	pF
Cout	Output Capacitance	V_{OUT} = GND	−	−	7	pF

AC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

READ CYCLE

SYMBOL	PARAMETER	−20		−25		−30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	−	25	−	30	−	ns
t_{AA}	Address Access Time	−	20	−	25	−	30	ns
t_{A12A}	A12 Access Time	−	15	−	17	−	20	ns
t_{LA}	ALE Access Time	−	20	−	25	−	30	ns
t_{CA}	$\overline{CE}$ Access Time	−	20	−	22	−	25	ns
t_{BA}	$\overline{BS}$ Access Time	−	20	−	22	−	25	ns
t_{OE}	$\overline{OE}$ Access Time	−	10	−	10	−	12	ns
t_{ASL}	Address Latch Set-Up Time	4	−	4	−	5	−	ns
t_{AHL}	Address Latch Hold Time	5	−	5	−	5	−	ns
t_{LP}	ALE Pulse Width	8	−	8	−	9	−	ns
t_{AOH}	Output Data Hold Time from Address Change	5	−	5	−	5	−	ns
t_{LOH}	Output Data Hold Time from Address Latch	5	−	5	−	5	−	ns
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	5	−	5	−	5	−	ns
t_{BLZ}	$\overline{BS}$ to Output in Low-Z	5	−	5	−	5	−	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	−	0	−	0	−	ns
t_{CHZ}	$\overline{CE}$ to Output in High-Z	−	10	−	10	−	12	ns
t_{BHZ}	$\overline{BS}$ to Output in High-Z	−	10	−	10	−	12	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	−	8	−	8	−	10	ns
t_{OOI}	$\overline{OEA}/\overline{OEB}$ Inhibit Time	8	−	8	−	10	−	ns

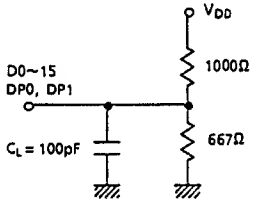
WRITE CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	-	25	-	30	-	ns
t_{WP}	$\overline{WE}$ Pulse Width	12	-	15	-	18	-	ns
t_{BW}	$\overline{BS}$ to End of Write	12	-	15	-	18	-	ns
t_{CW}	$\overline{CE}$ to End of Write	12	-	15	-	18	-	ns
t_{AW}	Write Address to End of Write	12	-	15	-	18	-	ns
t_{A12W}	Write Address A12 to End of Write	12	-	15	-	18	-	ns
t_{AS}	Write Address Set-Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{DS}	Data Set-Up Time	8	-	10	-	10	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	-	5	-	5	-	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	7	-	8	-	10	ns
t_{OEH}	$\overline{OE}$ Command Hold Time	5	-	5	-	5	-	ns
t_{WEH}	$\overline{WE}$ Command Hold Time	-	5	-	5	-	5	ns
t_{WI}	Write Command Inhibit Time	10	-	10	-	10	-	ns
t_{WA}	$\overline{WE}$ Access Time	-	20	-	25	-	30	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

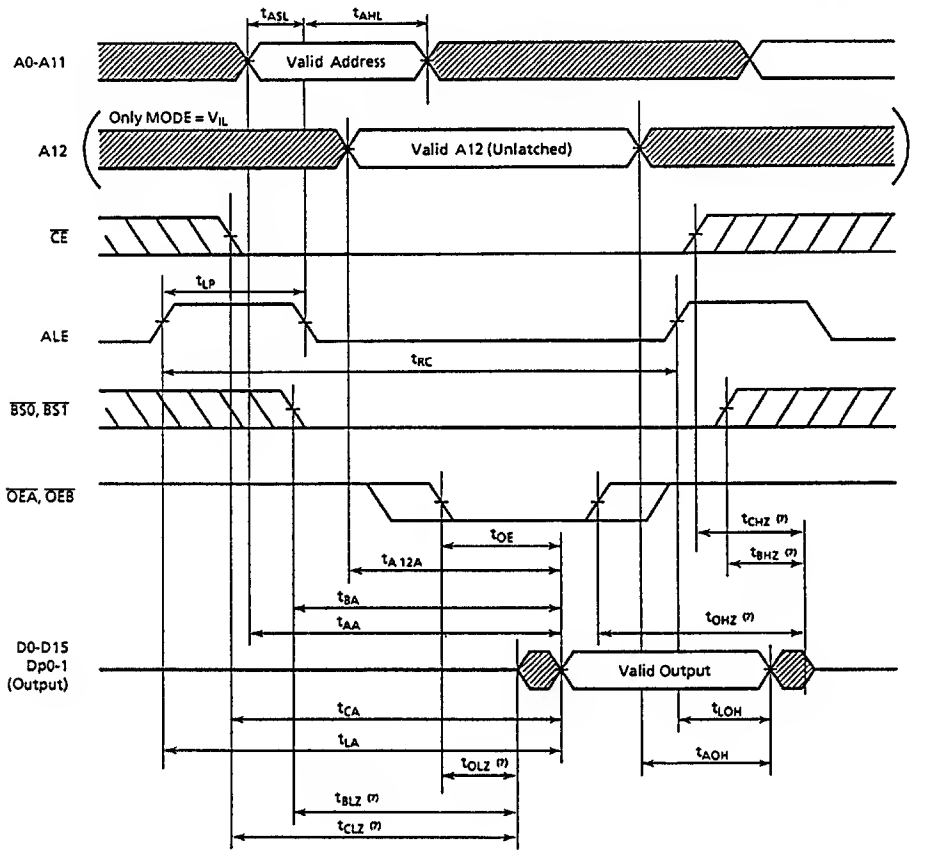
Fig. 1 OUTPUT LOAD



TIMING WAVEFORMS

READ CYCLE TIMING 1

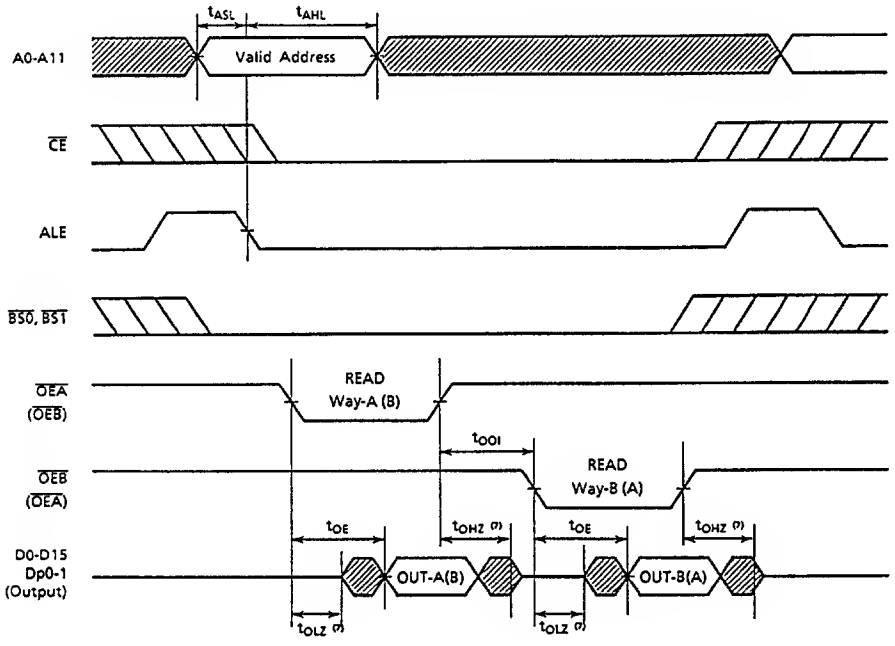
MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

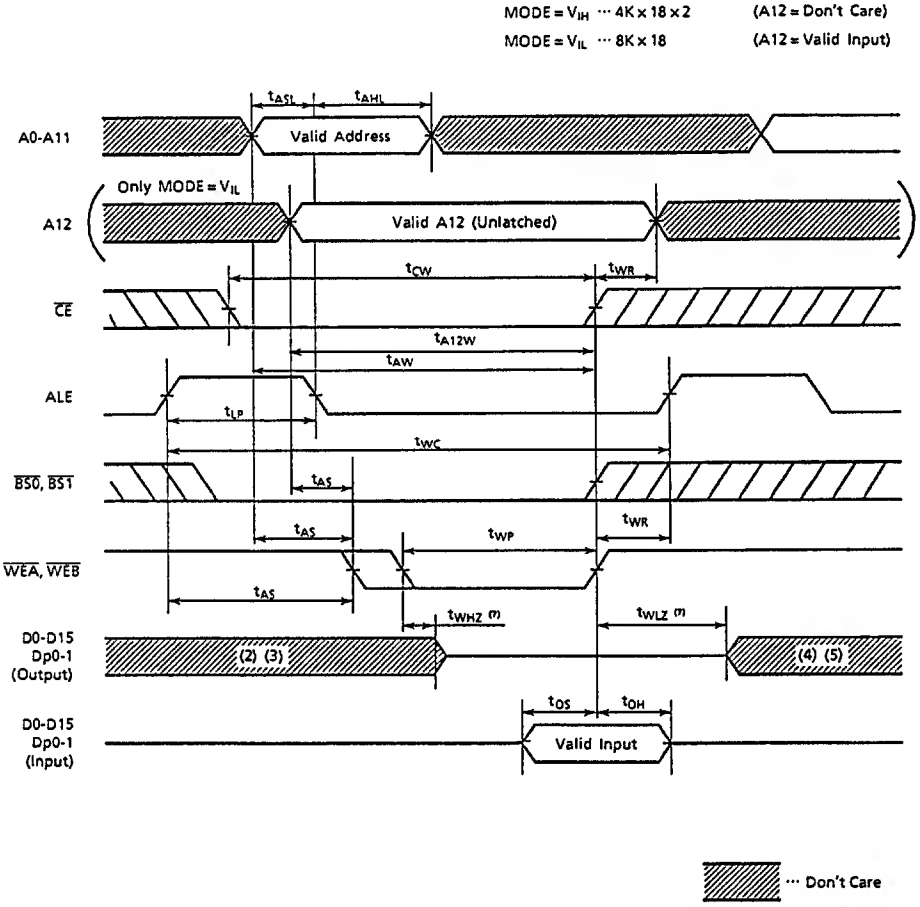
READ CYCLE TIMING 2 (t_{OOI} TIMING . MODE = V_{IH})



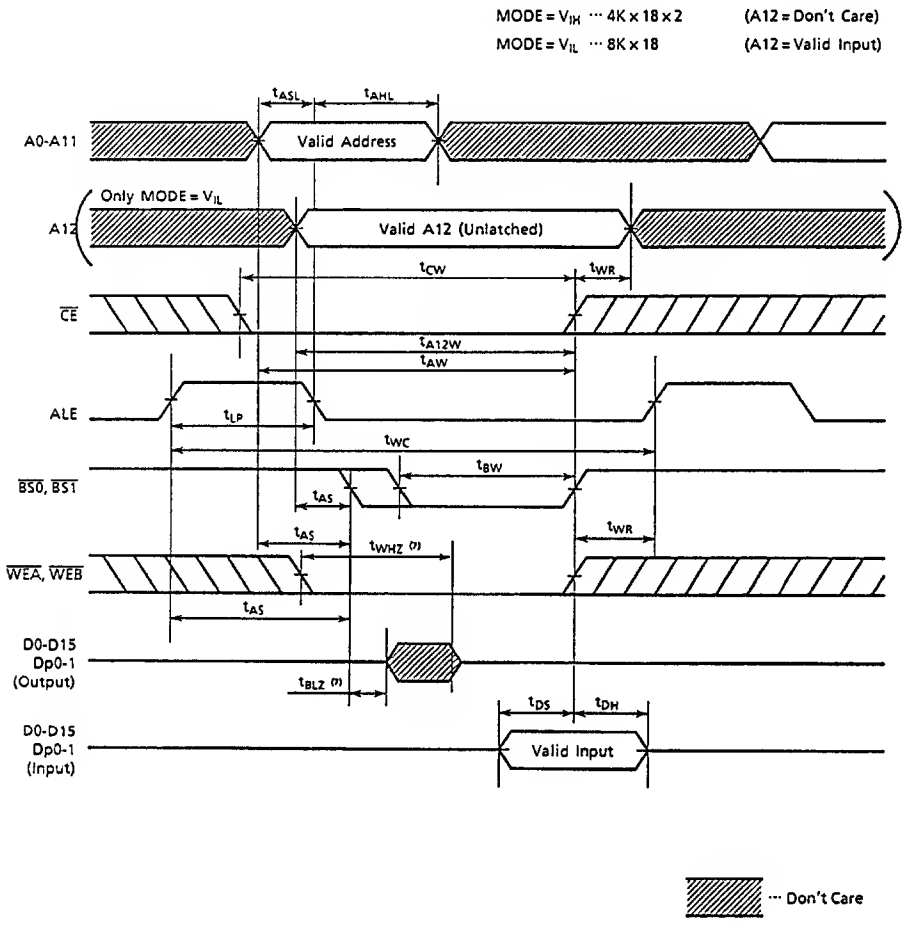
NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

WRITE CYCLE TIMING 1 ($\overline{WE}$ Control) (6)

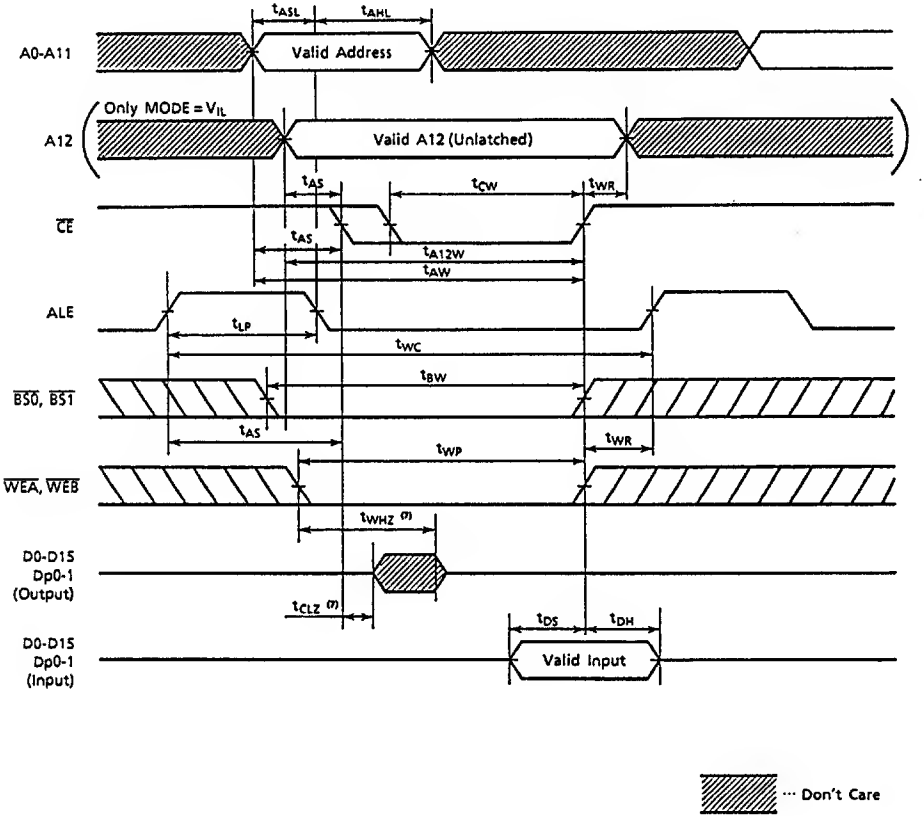


WRITE CYCLE TIMING 2 ($\overline{BS}$ Control) (6)

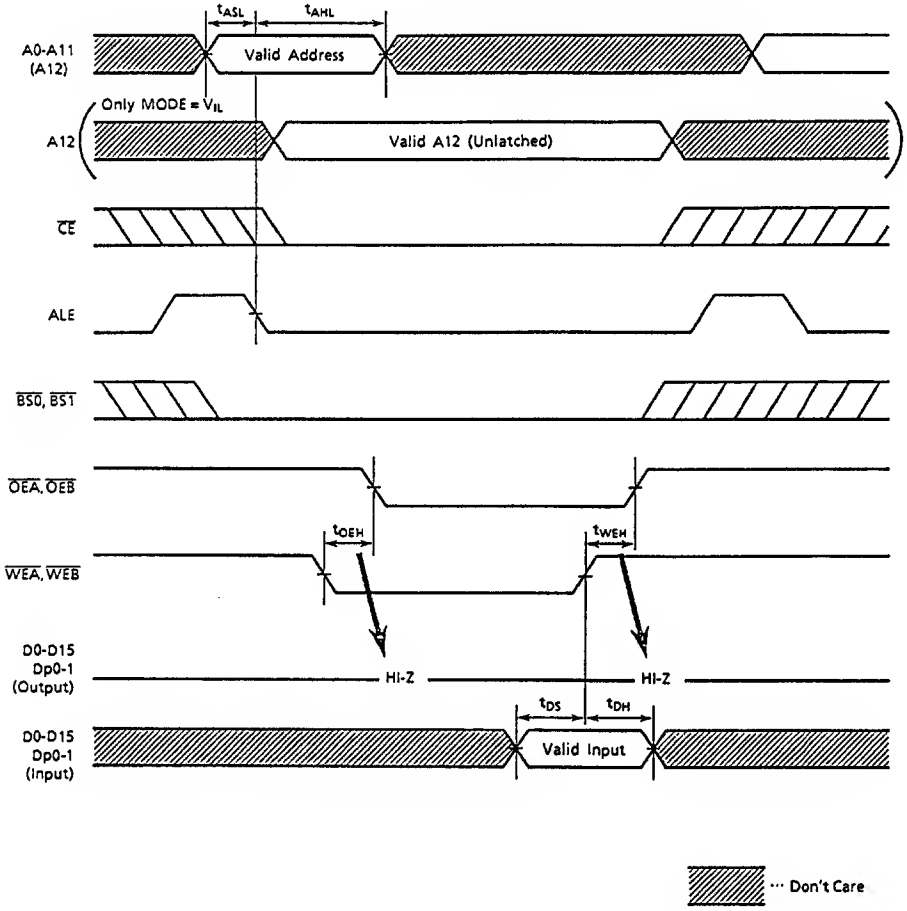


WRITE CYCLE TIMING 3 ($\overline{CE}$ Control) (6)

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)

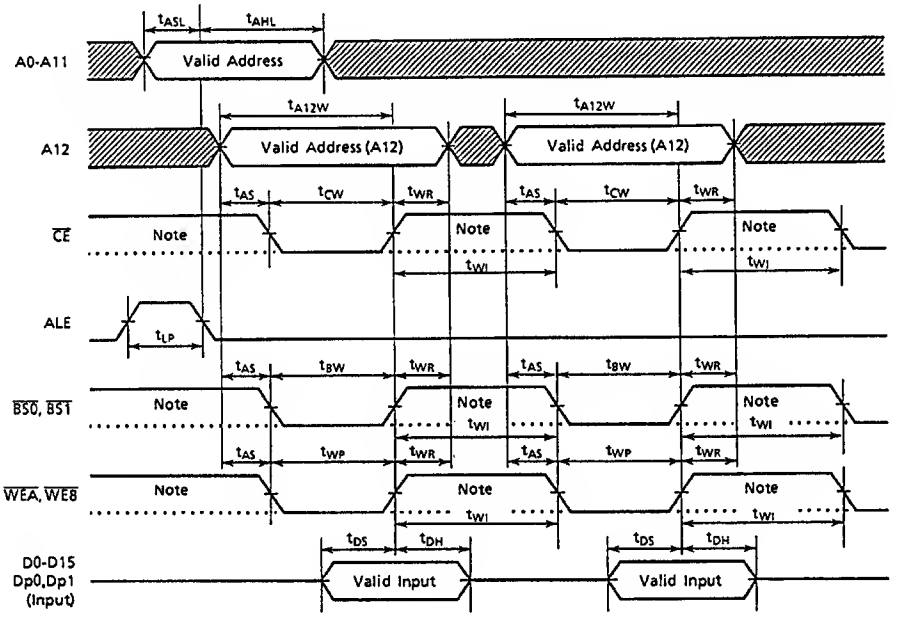


WRITE CYCLE TIMING 4 (t_{OEH} and t_{WEH}) (6)



WRITE CYCLE TIMING 5 (A12 Control) (6)

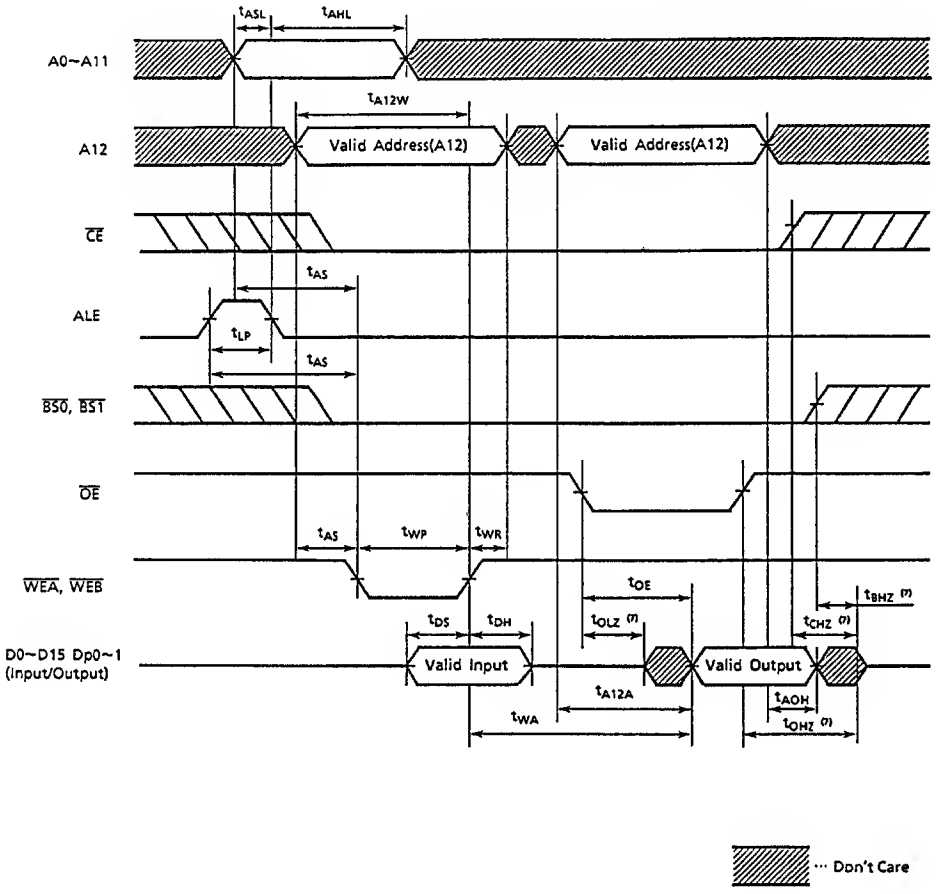
Only MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



Note ; t_{WI} ··· Write Command Inhibit Time
($\overline{CE}$ = H or $\overline{BS0}$ = $\overline{BS1}$ = H or $\overline{WEA}$ = $\overline{WEB}$ = H)

··· Don't Care

READ AFTER WRITE CYCLE TIMING



NOTE : 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{BS0}$ or $\overline{BS1}$ Low transition occur coincident with or after $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

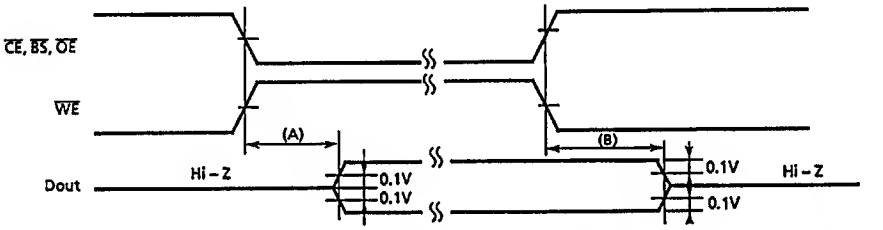
5. Assuming that $\overline{BS0}$ or $\overline{BS1}$ High transition occurs coincident with or prior to $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

6. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

7. These parameters are specified as follows and measured by using load shown in Fig. 1.

(A) t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{WLZ} ··· Output Enable Time

(B) t_{CHZ}, t_{BHZ}, t_{OHZ}, t_{WHZ} ··· Output Disable Time



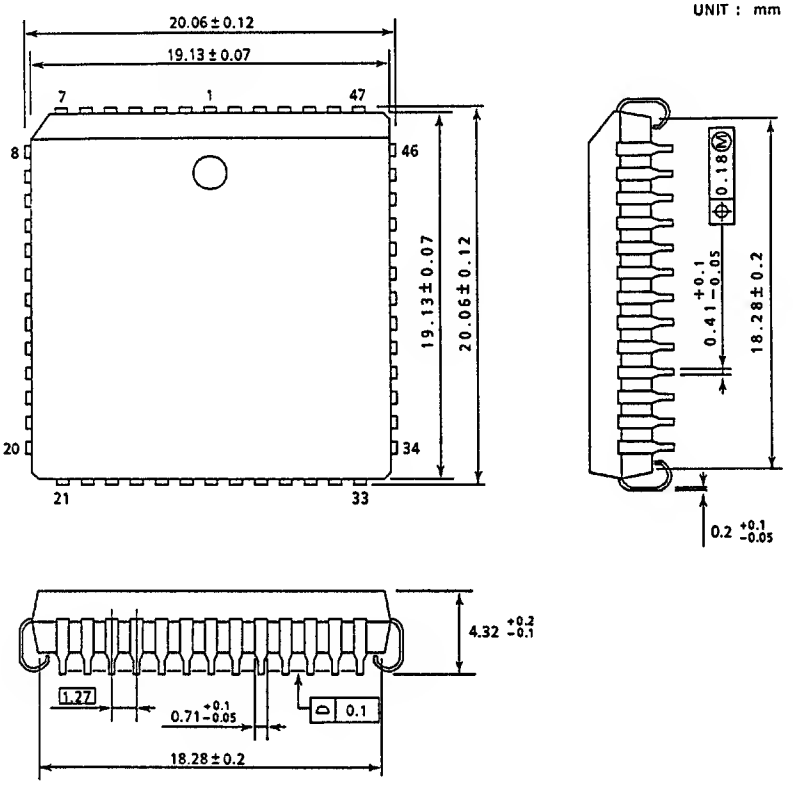
8. The Write Data and Write Address are indeterminate when the input level of $\overline{WEA}$ and $\overline{WEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

9. The Read Data are indeterminate when the input level of $\overline{OEA}$ and $\overline{OEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

OUTLINE DRAWING

QFJ52−P−S750

UNIT : mm



Weight : 2.68g (Typ.)

2-WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS
CMOS STATIC CACHE DATA RAM

DESCRIPTION

The TC55188T is a 147,456bits high-speed static RAM which can be user-configured either as 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with a byte control, on-chip address latches and chip-enable latch. The TC55188T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed feature, and is operated from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolar TTL circuits. The TC55188T can directly interface with the INTEL 82385 cache controller, without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore; Significant reductions in the number of parts, board assembly area and power dissipation can be achieved by using the TC55188T cache data RAM. The MODE input of the TC55188T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bits organization which is suitable for 2-way set associative cache designs or as a 8,192 words by 18 bits organization suitable for direct map cache designs. The TC55188T can also be operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55188T is packaged in a 52-pin standard PLCC for high-density board level assembly.

FEATURES

- Fast Access Time (max.)

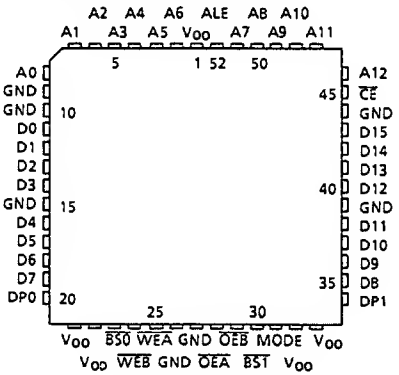
ITEM		TC55188T		
		-20	-25	-30
t_{RC}	Cycle Time	20ns	25ns	30ns
t_{AA}	Address Access Time	20ns	25ns	30ns
t_{OE}	$\overline{OE}$ Access Time	10ns	10ns	12ns

- Power dissipation
  - Operating TC55188T-20 230mA (max.)
    TC55188T-25 220mA (max.)
    TC55188T-30 200mA (max.)
  - Standby 40mA (max.)
- Configurable for 2-way or direct RAM arrays
  2-way 4,096words×18bits (MODE = V_{IH})
  8,192words×18bits (MODE = V_{IL})
- Contains address latches, $\overline{CE}$ latch and byte control, $\overline{BS0}$ and $\overline{BS1}$
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V ± 10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : $\overline{OEA}$, $\overline{OEB}$
- Two Write enable controls : $\overline{WEA}$, $\overline{WEB}$
- TC55188T : QFJ-P-S750

PIN NAMES

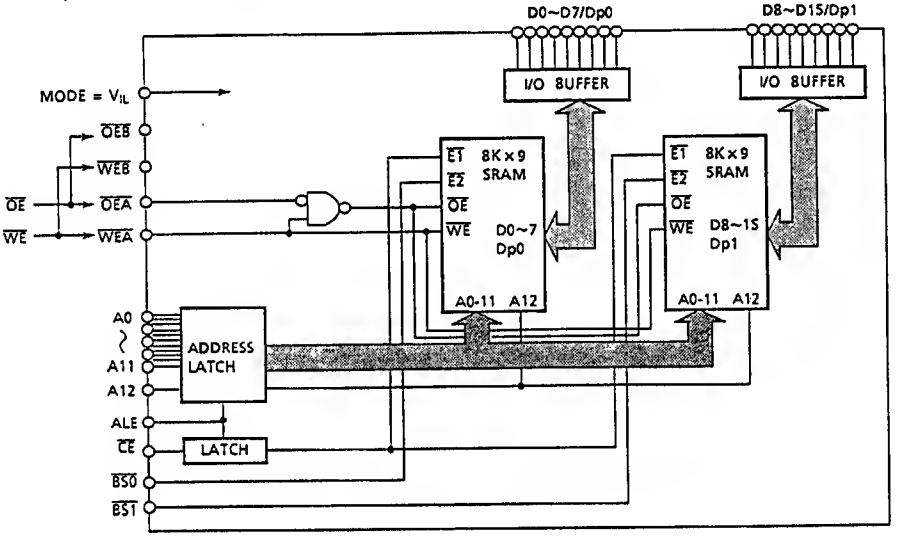
A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input/Output
ALE	Address/$\overline{CE}$ Latch Input
$\overline{CE}$	Chip Enable Input
$\overline{BS0}$	Lower Byte Select Input
$\overline{BS1}$	Upper Byte Select input
$\overline{OEA}$	Output Enable Input (Way-A)
$\overline{OEB}$	Output Enable Input (Way-B)
$\overline{WEA}$	Write Enable Input (Way-A)
$\overline{WEB}$	Write Enable Input (Way-B)
MODE	Mode Select Input
VDD	Power (+5V)
GND	Ground

PIN CONNECTION (TOP VIEW)

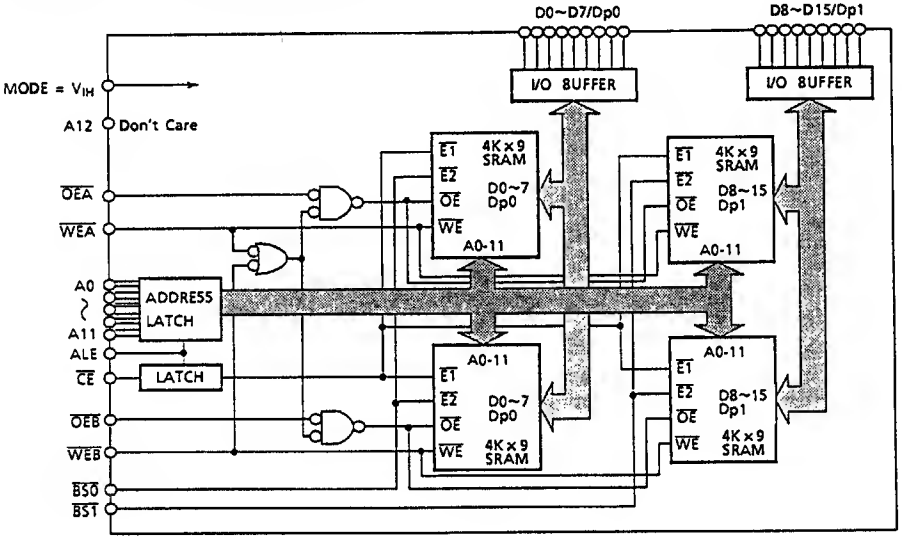


BLOCK DIAGRAM

1−WAY 8,192 words × 18 bits (MODE : V_{IL})



2−WAY 4,096 words × 18 bits (MODE : V_{IH})



TRUTH TABLE 1

CONTROL INPUT			FUNCTION			CONFIGURATION
MODE	ALE	$\overline{CE}$	CHIP	A0~A11	A12	
H	H	H	Disable	*1	*1	4K × 18 × 2
H	H	L	Enable	Valid	*1	
H	L	H*2	Disable	Latched	Latched	
H	L	L*2	Enable	Latched	Latched	
L	H	H	Disable	*1	*1	8K × 18
L	H	L	Enable	Valid	Valid	
L	L	H*2	Disable	Latched	Latched	
L	L	L*2	Enable	Latched	Latched	

*1 : Don't Care *2 : Latched level as ALE from H to L

TRUTH TABLE 2 (MODE = V_{IL} ··· 8K × 18)

INPUTS						OPERATION		
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	CHIP	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	H	L	H	L	H	Undefine (9)	Undefine	Undefine
				H	L			
				L	L			
H	L	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			
L	H	*	*	L	H	Undefine (8)	Undefine	Undefine
				H	L			
				L	L			

* : H or L

TRUTH TABLE 3 (MODE = V_{IH} ··· 4K x 18 x 2)

INPUTS						OPERATION			
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	way-A	way-B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way-B Output	Open
				H	L			Open	way-B Output
				L	L			way-B Output	way-B Output
H	H	L	H	L	H	Read Cycle	Deselect	way-A Output	Open
				H	L			Open	way-A Output
				L	L			way-A Output	way-A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way-B Input	Open
				H	L			Open	way-B Input
				L	L			way-B Input	way-B Input
L	H	*	*	L	H	Write Cycle	Deselect	way-A Input	Open
				H	L			Open	way-A Input
				L	L			way-A Input	way-A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way-A/B Input	Open
				H	L			Open	way-A/B Input
				L	L			way-A/B Input	way-A/B Input

*: Don't Care

MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.3	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C) (1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : -3V pulse width less than 10ns.

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		-1	-	+1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	Output Disable		-1	-	+1	μA
I_{DDO}	Operating Current	t_{RC}, t_{WC} = min. cycle Add., $\overline{WE}$, ALE = Clock (3V/0V) $\overline{OE}$ = 3.0V $\overline{CE}$, $\overline{BS}$ = 0V, MODE = 3.0V/0V	-20	-	-	230	mA
			-25	-	-	220	
			-30	-	-	200	
I_{DDS}	Standby Current	$\overline{CE}$, $\overline{BS}$, $\overline{WE}$, $\overline{OE}$ = V_{IH}, ALE = V_{IL} Add., Data, MODE = V_{IH} or V_{IL}		-	-	40	mA

CAPACITANCE (Ta = 25°C, freq. = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cin	Input Capacitance	V_{IN} = GND	-	-	5	pF
Cout	Output Capacitance	V_{OUT} = GND	-	-	7	pF

AC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%) (1)

READ CYCLE

SYMBOL	PARAMETER	−20		−25		−30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	−	25	−	30	−	ns
t_{AA}	Address Access Time	−	20	−	25	−	30	ns
t_{LA}	ALE Access Time	−	20	−	25	−	30	ns
t_{CA}	$\overline{CE}$ Access Time	−	20	−	22	−	25	ns
t_{BA}	$\overline{BS}$ Access Time	−	20	−	22	−	25	ns
t_{OE}	$\overline{OE}$ Access Time	−	10	−	10	−	12	ns
t_{ASL}	Address Latch Set-Up Time	4	−	4	−	5	−	ns
t_{AHL}	Address Latch Hold Time	5	−	5	−	5	−	ns
t_{LP}	ALE Pulse Width	8	−	8	−	9	−	ns
t_{AOH}	Output Data Hold Time from Address Change	5	−	5	−	5	−	ns
t_{LOH}	Output Data Hold Time from Address Latch	5	−	5	−	5	−	ns
t_{LLZ}	ALE to Output in Low − Z	5	−	5	−	5	−	ns
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	5	−	5	−	5	−	ns
t_{BLZ}	$\overline{BS}$ to Output in Low-Z	5	−	5	−	5	−	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	−	0	−	0	−	ns
t_{LHZ}	ALE to Output in High − Z	−	12	−	12	−	15	ns
t_{CHZ}	$\overline{CE}$ to Output in High-Z	−	10	−	10	−	12	ns
t_{BHZ}	$\overline{BS}$ to Output in High-Z	−	10	−	10	−	12	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	−	8	−	8	−	10	ns
t_{OOI}	$\overline{OEA}/\overline{OEB}$ Inhibit Time	8	−	8	−	10	−	ns

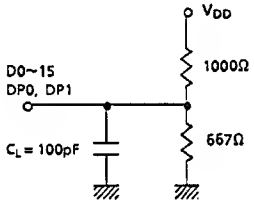
WRITE CYCLE

SYMBOL	PARAMETER	−20		−25		−30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	−	25	−	30	−	ns
t_{WP}	$\overline{WE}$ Pulse Width	12	−	15	−	18	−	ns
t_{BW}	$\overline{BS}$ to End of Write	12	−	15	−	18	−	ns
t_{CW}	$\overline{CE}$ to End of Write	12	−	15	−	18	−	ns
t_{AW}	Write Address to End of Write	12	−	15	−	18	−	ns
t_{AS}	Write Address Set-Up Time	0	−	0	−	0	−	ns
t_{WR}	Write Recovery Time	0	−	0	−	0	−	ns
t_{DS}	Data Set-Up Time	8	−	10	−	10	−	ns
t_{DH}	Data Hold Time	0	−	0	−	0	−	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	−	5	−	5	−	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	−	7	−	8	−	10	ns
t_{OEH}	$\overline{OE}$ Command Hold Time	5	−	5	−	5	−	ns
t_{WEH}	$\overline{WE}$ Command Hold Time	−	5	−	5	−	5	ns
t_{WI}	Write Command Inhibit Time	10	−	10	−	10	−	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

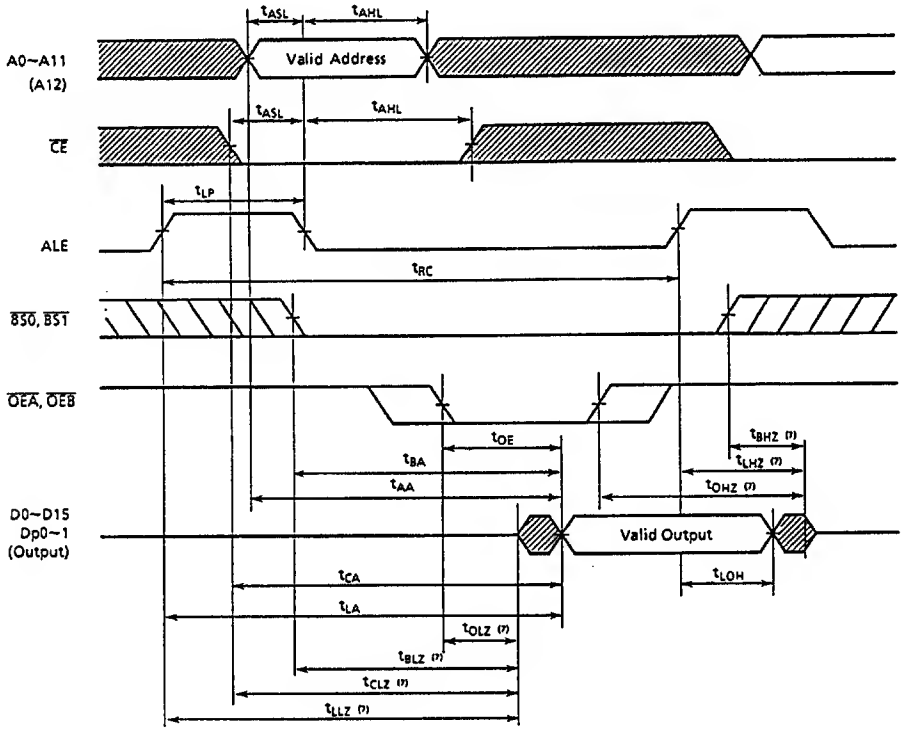
Fig. 1 OUTPUT LOAD



TIMING WAVEFORMS

READ CYCLE TIMING 1 (ALE=Clock)

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)

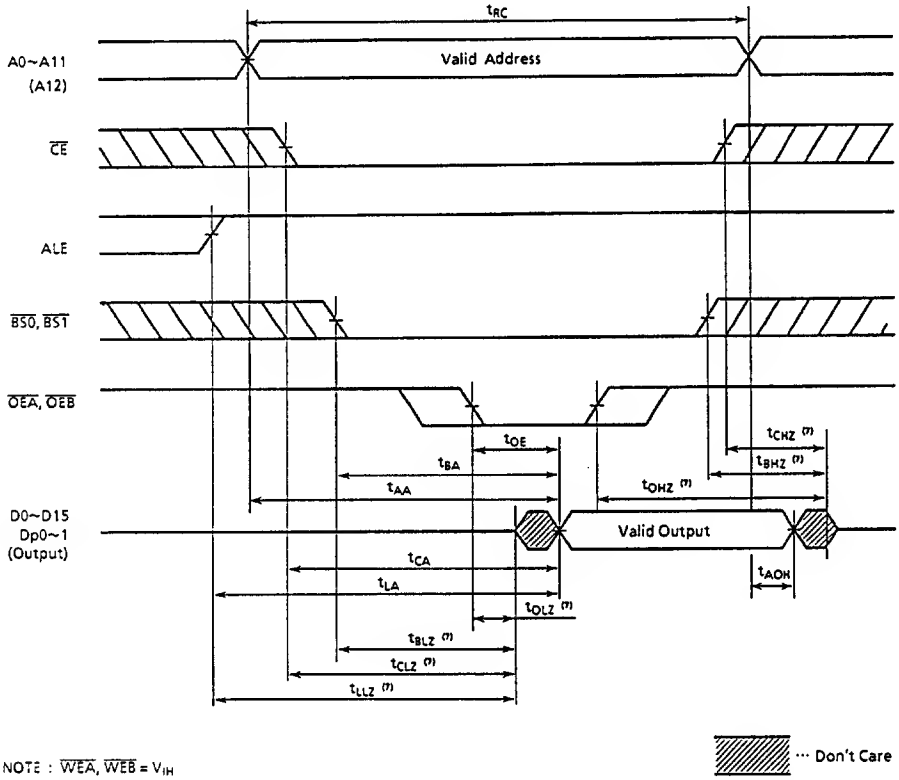


NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

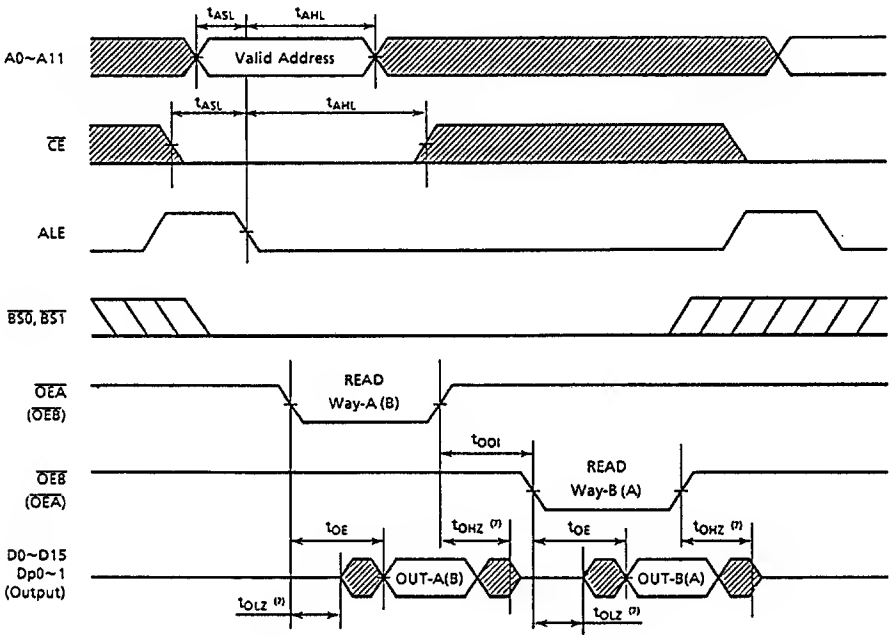
READ CYCLE TIMING 2 (ALE = V_{IH})

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

READ CYCLE TIMING 3 (t_{OOI} TIMING . MODE = V_{IH})

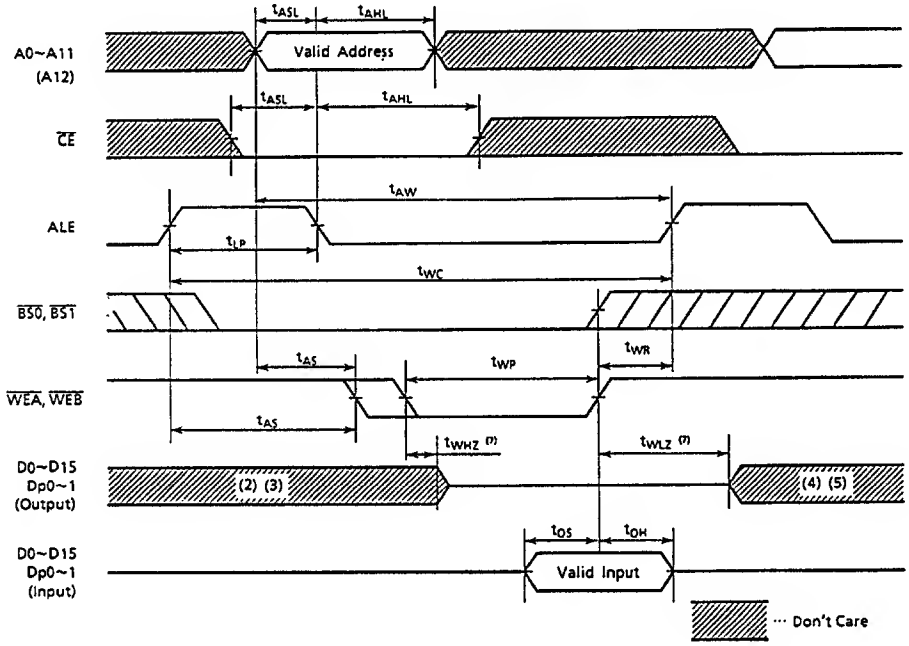


NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

··· Don't Care

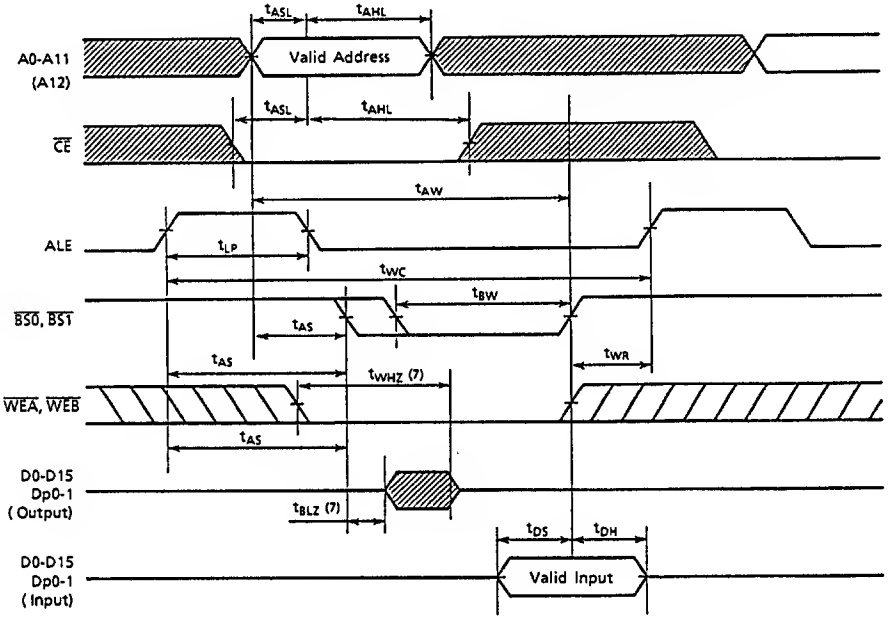
WRITE CYCLE TIMING 1 ($\overline{WE}$ Control) (6)

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



WRITE CYCLE TIMING 2 ($\overline{BS}$ Control) (6)

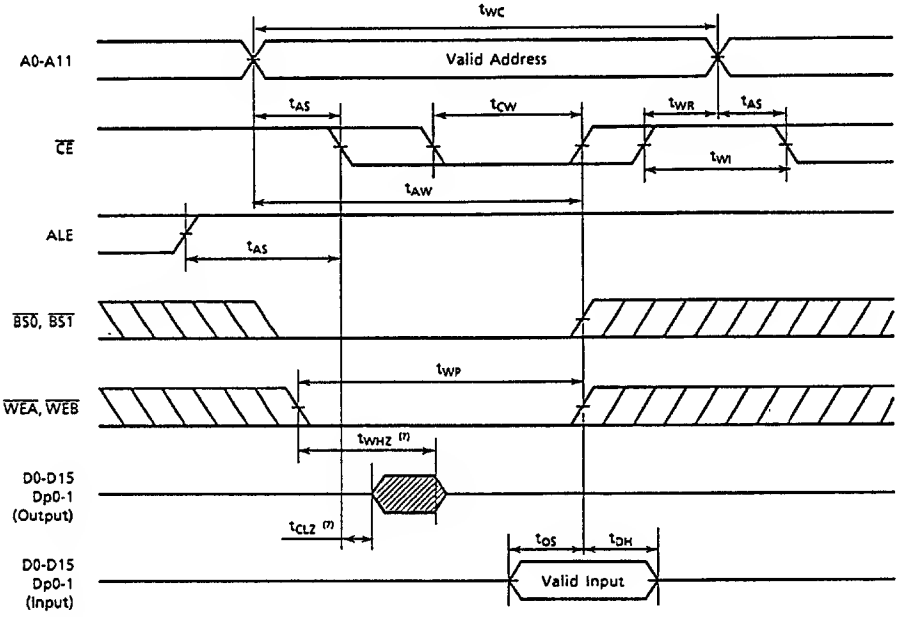
MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



··· Don't Care

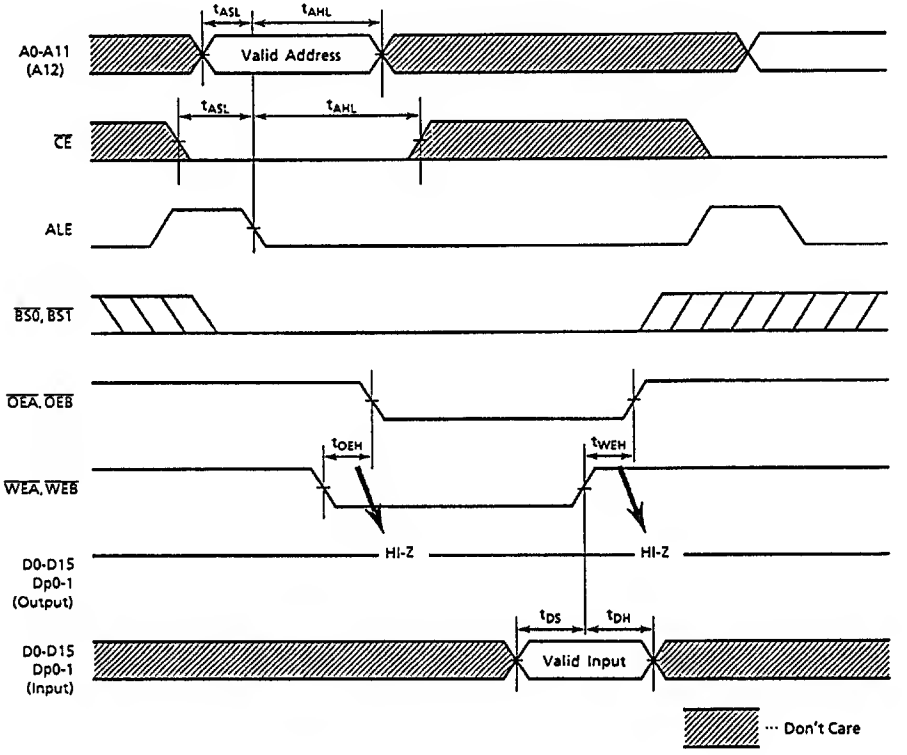
WRITE CYCLE TIMING 3 ($\overline{CE}$ Control) (6)

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



··· Don't Care

WRITE CYCLE TIMING 4 (t_{OEH} and t_{WEH}) [6]



NOTE : 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{BS0}$ or $\overline{BS1}$ Low transition occur coincident with or after $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

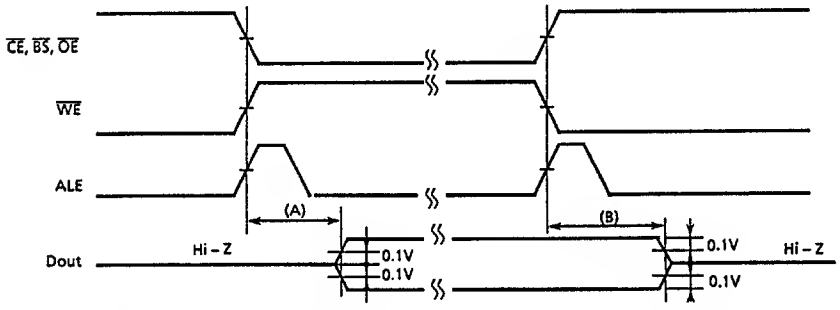
5. Assuming that $\overline{BS0}$ or $\overline{BS1}$ High transition occurs coincident with or prior to $\overline{WE}$ transition, Lower Byte Outputs (D0~D7, Dp0) or Upper Byte Outputs (D8~D15, Dp1) remain in a high impedance state.

6. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

7. These parameters are specified as follows and measured by using load shown in Fig. 1.

(A) t_{LLZ}, t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{WLZ} ··· Output Enable Time

(B) t_{LHZ}, t_{CHZ}, t_{BHZ}, t_{OHZ}, t_{WHZ} ··· Output Disable Time



* The relation between signals depends on the preceding Timing Charts.

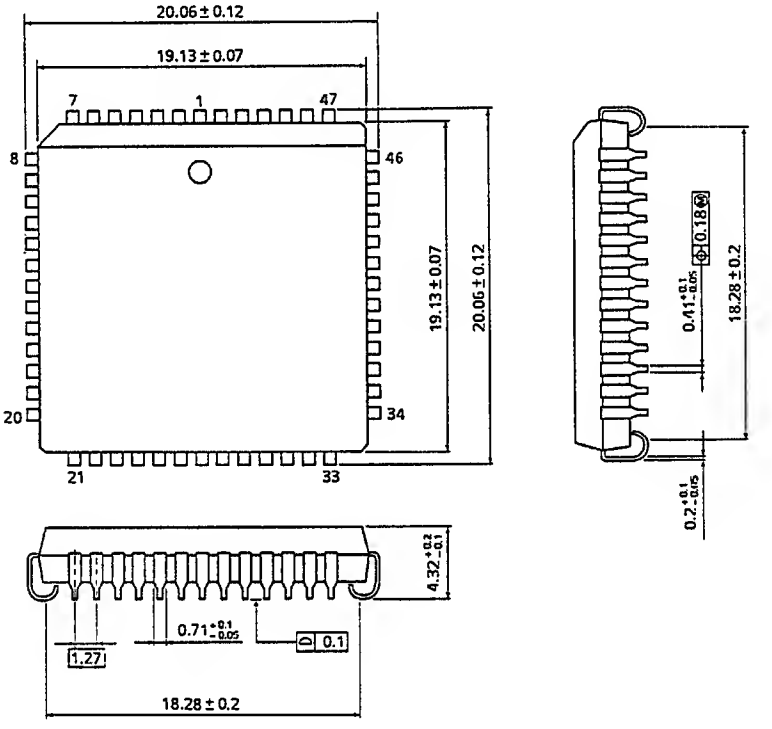
8. The Write Data and Write Address are indeterminate when the input level of $\overline{WEA}$ and $\overline{WEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

9. The Read Data are indeterminate when the input level of $\overline{OEA}$ and $\overline{OEB}$ is diferent on Direct Mapping Mode (MODE = V_{IL}).

OUTLINE DRAWING

QFJ52−P−S750

UNIT : mm



Weight : 2.68g (Typ.)

65,536 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55464P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55464P/J has low power feature with device control using Chip Enable ($\overline{CE}$). Also the device power at memory access is reduced by automatic power down circuit form.

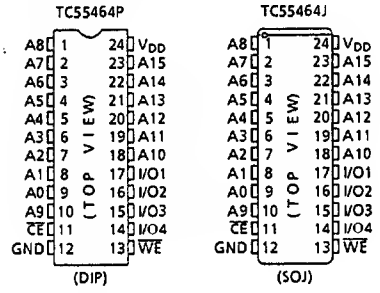
The TC55464P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55464P/J is packaged in a 24 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

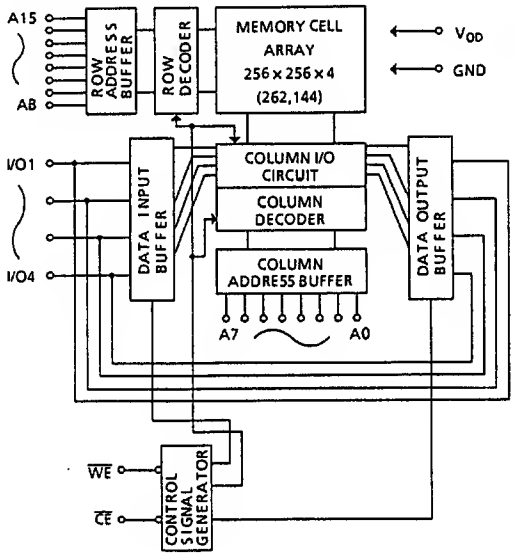
FEATURES

- Fast access time :
  - TC55464P/J-17 17ns(MAX.)
  - TC55464P/J-20 20ns(MAX.)
  - TC55464P/J-25 25ns(MAX.)
  - TC55464P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55464P/J-17 120mA(MAX.)
  - TC55464P/J-20 120mA(MAX.)
  - TC55464P/J-25 120mA(MAX.)
  - TC55464P/J-35 100mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - -17 : 5V±5%
  - -20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package TC55464P : DIP24-P-300B
  TC55464J : SOJ24-P-300A

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power(+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-17	4.75	5.0	5.25	V
		-20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		-0.5*	-	0.8	V

* -3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			-	-	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			-	-	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE}$ = V_{IL} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	-17	-	-	120	mA
			V_{DD} = 5.5V	-20	-	-	120	
				-25	-	-	120	
				-35	-	-	100	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE}$ = V_{IH} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	-17	-	-	20	mA
			V_{DD} = 5.5V	-20				
				-25				
				-35				
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V or 0.2V			-	-	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ (1), $-17: V_{DD} = 5V \pm 5\%$, $-20/25/35: V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	17	–	20	–	25	–	35	ns
t_{CO}	$\overline{CE}$ Access Time	–	17	–	20	–	25	–	35	ns
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COO}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	–	15	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	17	–	20	–	25	–	35	ns

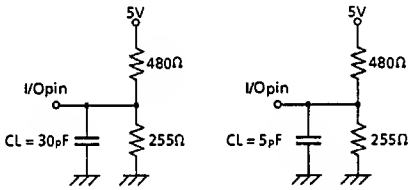
WRITE CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	13	–	13	–	15	–	20	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13	–	13	–	15	–	20	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set Up Time	10	–	10	–	12	–	15	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{OOW}	Output Disable Time from $\overline{WE}$	–	B	–	8	–	10	–	15	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

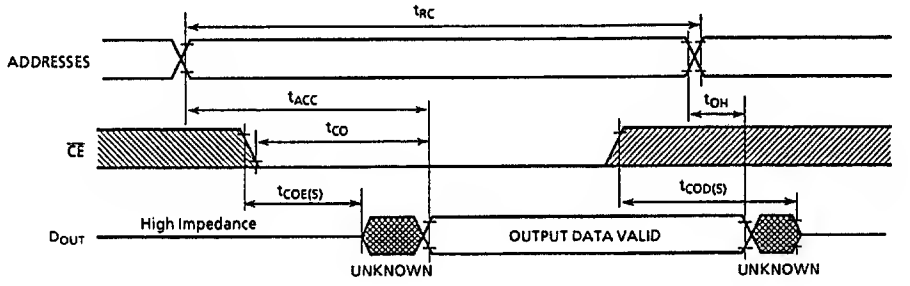
Fig. 1



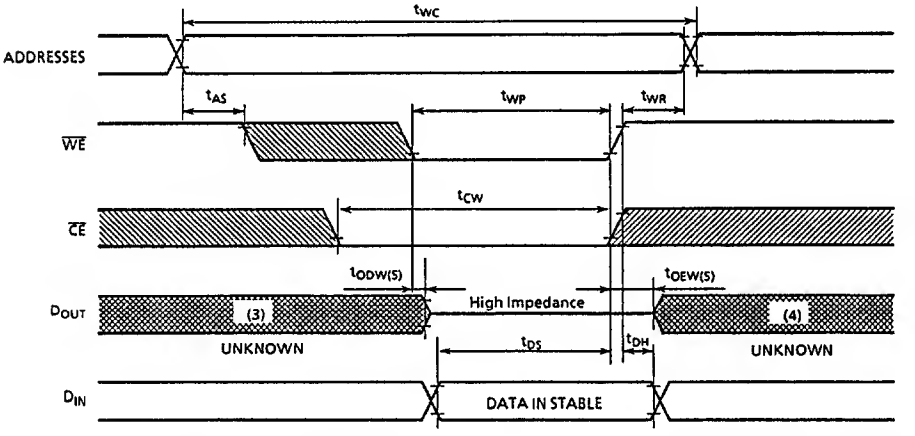
(For t_{COE}, t_{COD}, t_{OEW} and t_{OOW})

TIMING WAVEFORMS

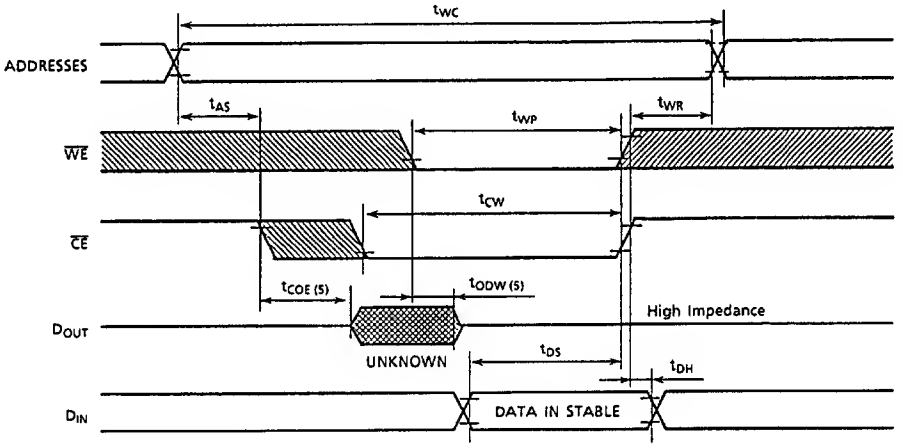
READ CYCLE (2)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



Note : 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

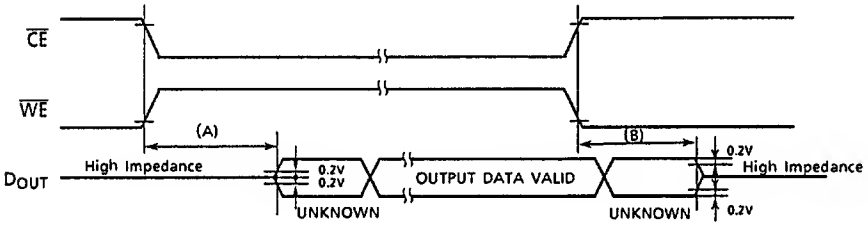
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEW} ····· Output Enable Time

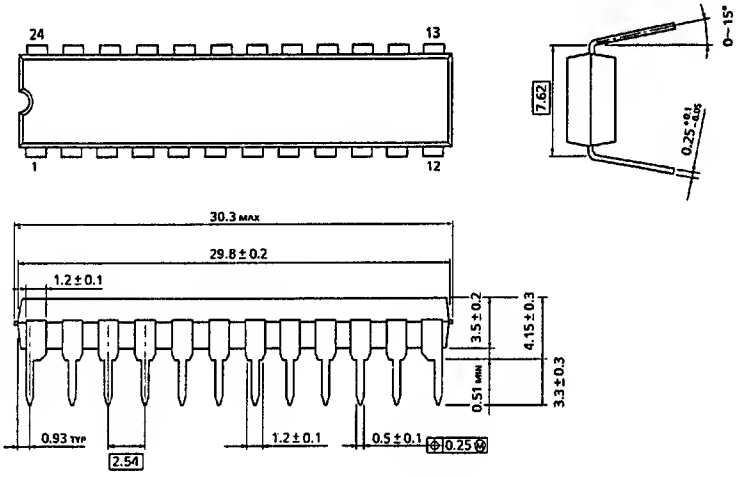
   (B) t_{COD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24 – P – 300B)

Unit : mm

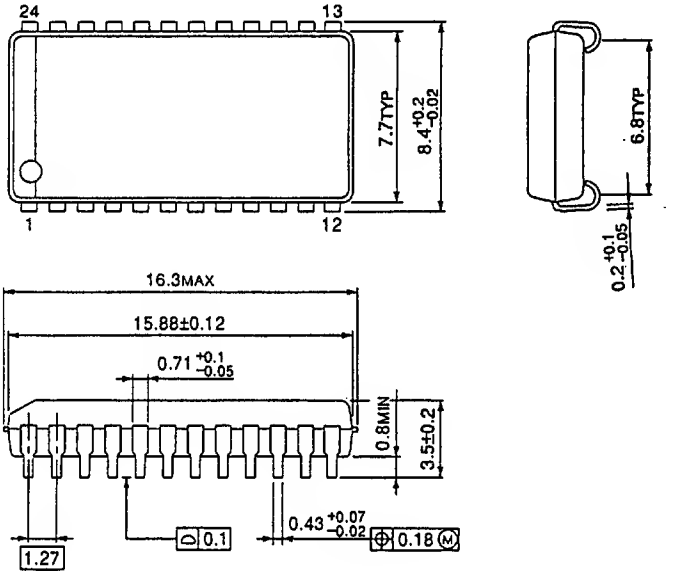


Weight : 1.72g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ24-P-300A)

Unit : mm



Weight : 0.72g (Typ.)

65,536 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55465P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55465P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

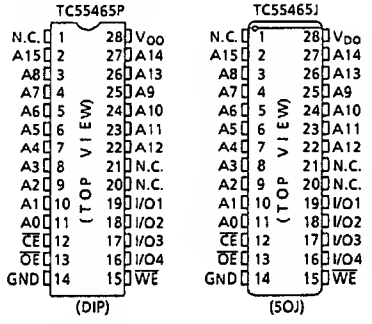
The TC55465P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55465P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

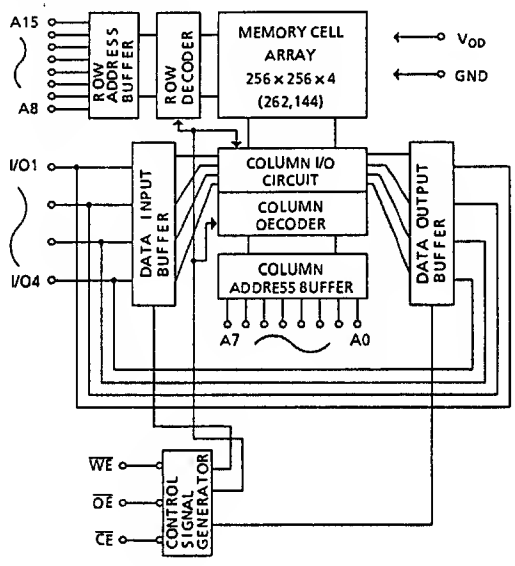
FEATURES

- Fast access time:
  - TC55465P/J-17 17ns(MAX.)
  - TC55465P/J-20 20ns(MAX.)
  - TC55465P/J-25 25ns(MAX.)
  - TC55465P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55465P/J-17 120mA(MAX.)
  - TC55465P/J-20 120mA(MAX.)
  - TC55465P/J-25 120mA(MAX.)
  - TC55465P/J-35 100mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55465P : DIP28−P−300B
  - TC55465J : SOJ28−P−300A

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0−A15	Address Inputs
I/01−I/04	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{OOO}	Operating Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	120	mA
		$\overline{CE}$ = V_{IL}	V_{DD} = 5.5V	−20	−	−	120	
		Other Input = V_{IH}/V_{IL}		−25	−	−	120	
				−35	−	−	100	
I_{DOS1}	Standby Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	20	mA
		$\overline{CE}$ = V_{IH}	V_{DD} = 5.5V	−20				
		Other Input = V_{IH}/V_{IL}		−25				
				−35				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (1), −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55465P/J-17		TC55465P/J-20		TC55465P/J-25		TC55465P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	17	–	20	–	25	–	35	ns
t_{CO}	$\overline{CE}$ Access Time	–	17	–	20	–	25	–	35	ns
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	15	ns
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	ns
t_{CDE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{CDO}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	–	15	ns
t_{DEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	ns
t_{DDD}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	10	–	15	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	17	–	20	–	25	–	35	ns

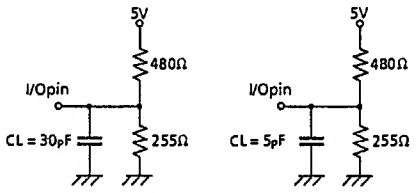
WRITE CYCLE

SYMBOL	PARAMETER	TC55465P/J-17		TC55465P/J-20		TC55465P/J-25		TC55465P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	13	–	13	–	15	–	20	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13	–	13	–	15	–	20	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set Up Time	10	–	10	–	12	–	15	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{DEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	10	–	15	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

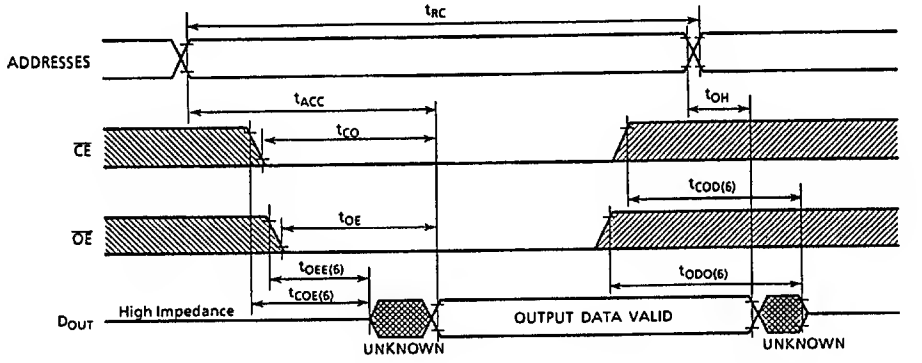
Fig. 1



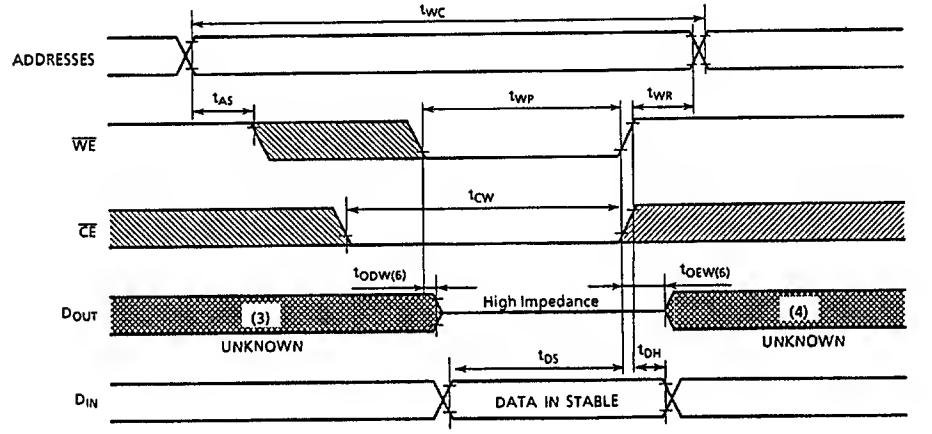
(For t_{CDE}, t_{OEE}, t_{CDD}, t_{DDD}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

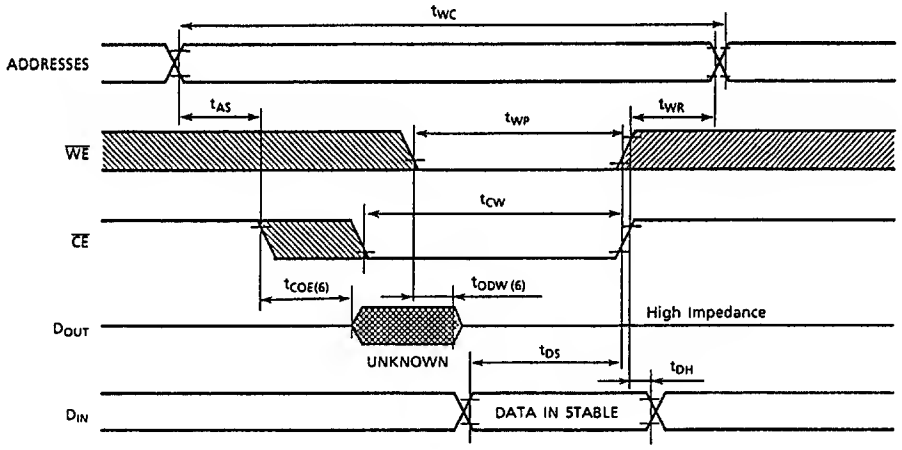
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

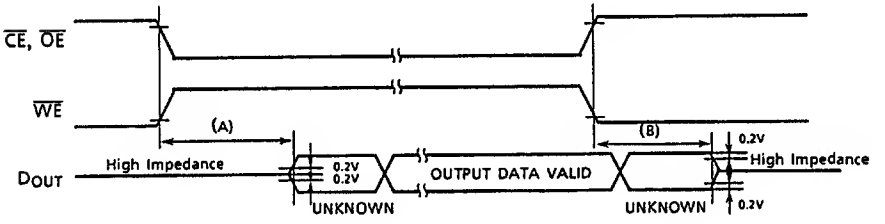
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enahle Time

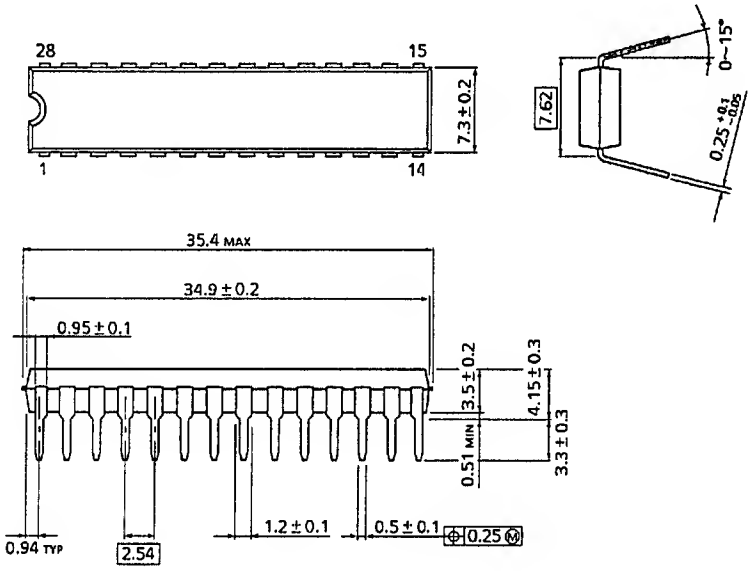
   (B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28 - P - 300B)

Unit in mm

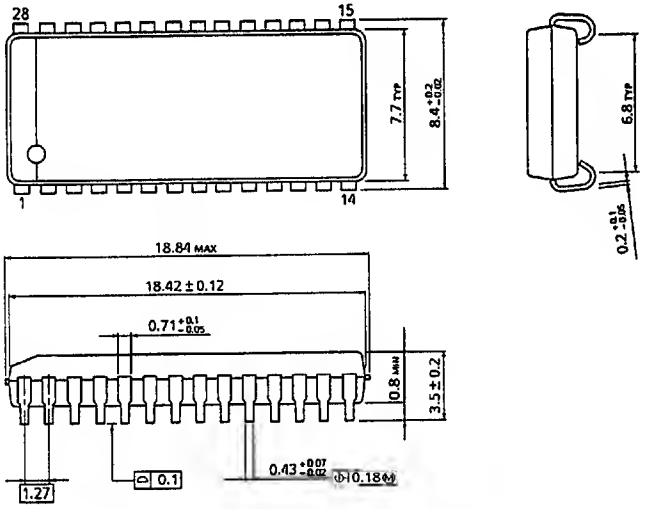


WEIGHT : 2.03g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28 – P – 300A)

UNIT : mm



WEIGHT : 0.83g (Typ.)

32,768 WORD × 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC55328P/J is a 262,144 bits high speed static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55328P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

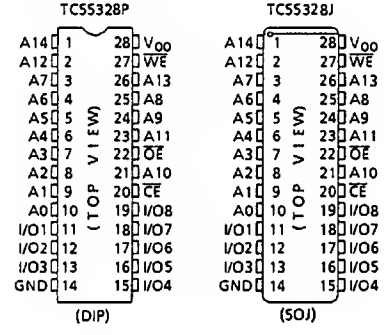
The TC55328P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55328P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

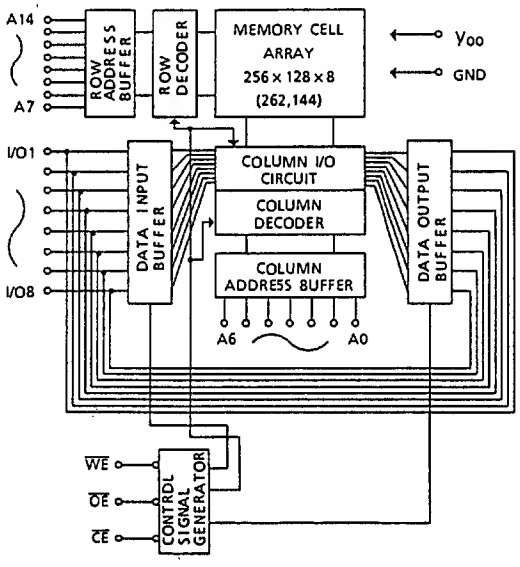
FEATURES

- Fast access time:
  - TC55328P/J-17 17ns(MAX.)
  - TC55328P/J-20 20ns(MAX.)
  - TC55328P/J-25 25ns(MAX.)
  - TC55328P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation: TC55328P/J-17 140mA(MAX.)
  - TC55328P/J-20 140mA(MAX.)
  - TC55328P/J-25 140mA(MAX.)
  - TC55328P/J-35 120mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package TC55328P : DIP28−P−300B
  - TC55328J : SOJ28−P−300A

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-17	4.75	5.0	5.25	V
		-20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		-0.5*	-	0.8	V

* -3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			-	-	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			-	-	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE}$ = V_{IL} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V V_{OO} = 5.5V	-17	-	-	140	mA
				-20	-	-	140	
				-25	-	-	140	
				-35	-	-	120	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE}$ = V_{IH} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V V_{DD} = 5.5V	-17	-	-	20	mA
				-20				
				-25				
				-35				
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Input = V_{OO} - 0.2V or 0.2V			-	-	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (1), -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	
t_{CO}	$\overline{CE}$ Access Time	-	17	-	20	-	25	-	35	
t_{OE}	$\overline{OE}$ Access Time	-	9	-	10	-	12	-	15	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t_{COE}	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	
t_{CDD}	Output Disable Time from $\overline{CE}$	-	10	-	10	-	10	-	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	0	-	
t_{ODD}	Output Disable Time from $\overline{OE}$	-	8	-	8	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	

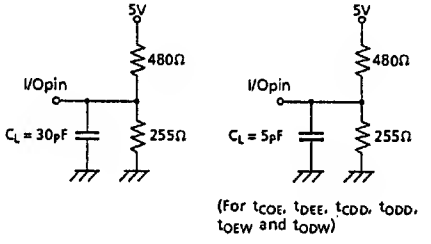
WRITE CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0		
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig.1

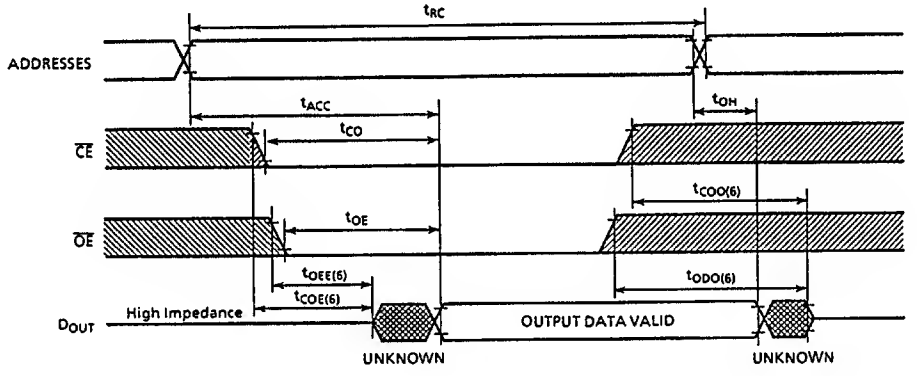
Fig.1



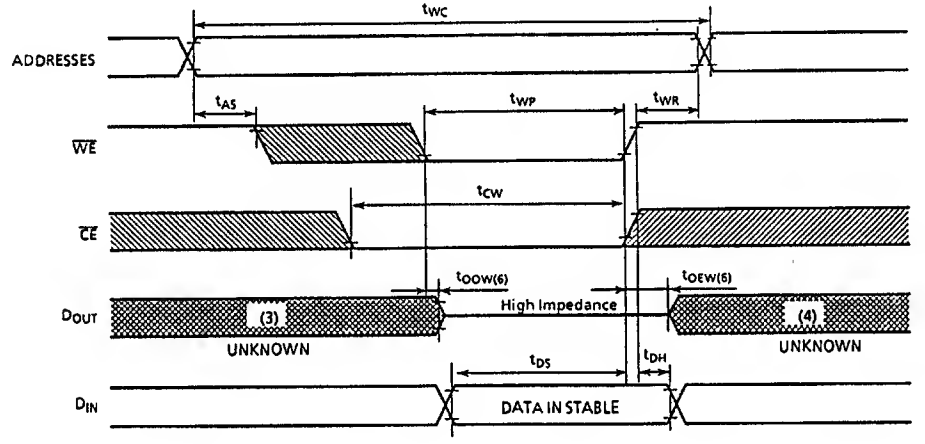
(For t_{COE}, t_{DEE}, t_{CDD}, t_{ODD}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

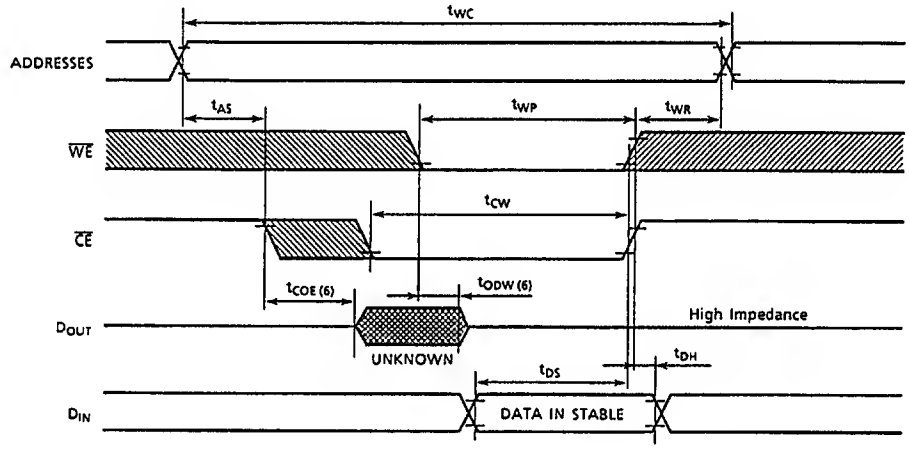
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

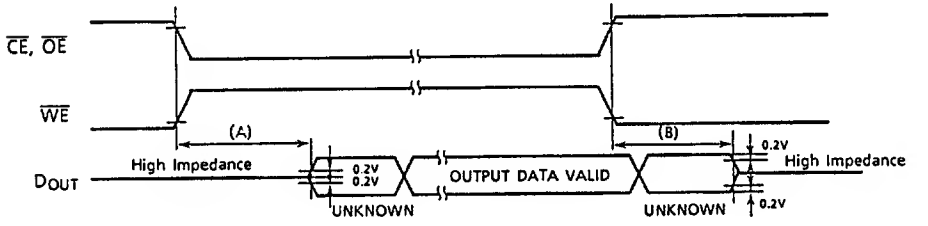
4 Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

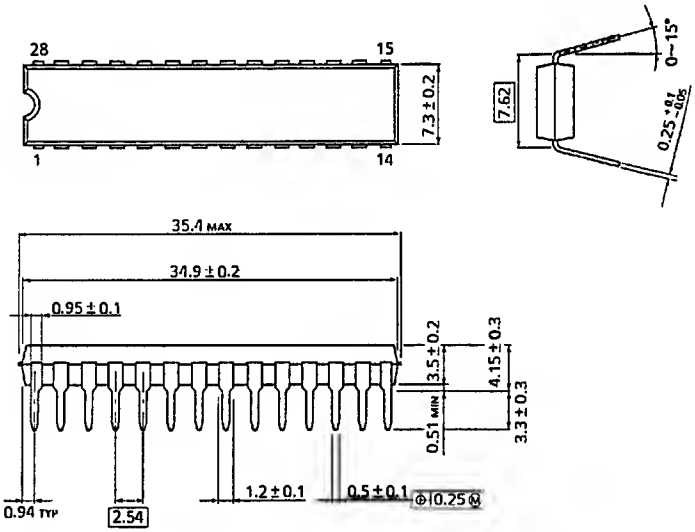
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28 - P - 300B)

UNIT in mm

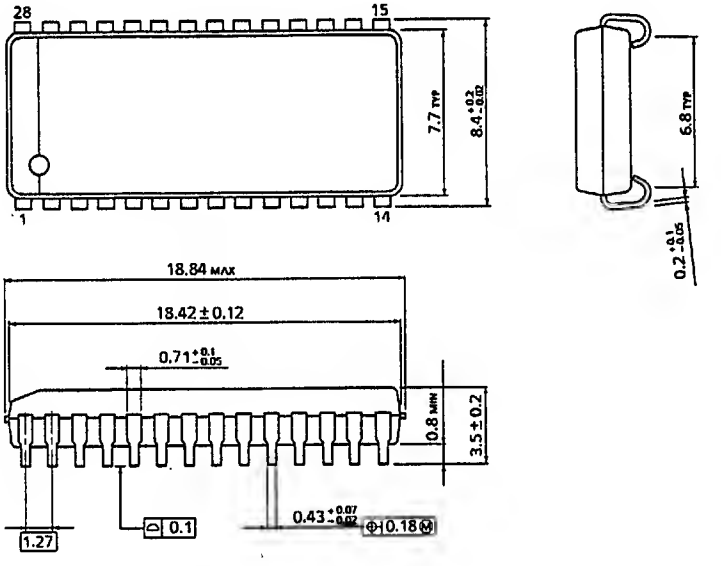


WEIGHT : 2.03g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28 – P – 300A)

UNIT in mm



WEIGHT : 0.83g (Typ.)

32,768 WORD × 9 BIT CMOS STATIC RAM

DESCRIPTION

The TC55329P/J is a 294,912 bits high speed static random access memory organized as 32,768 words by 9 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55329P/J has low power feature with device control using Chip Enable ($\overline{CE1}$/CE2), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

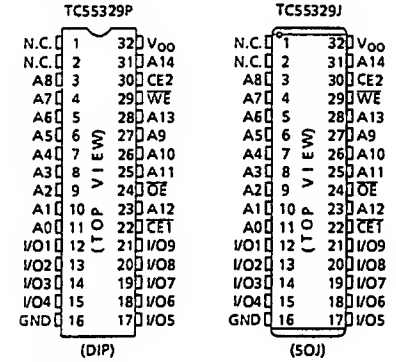
The TC55329P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55329P/J is packaged in a 32 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

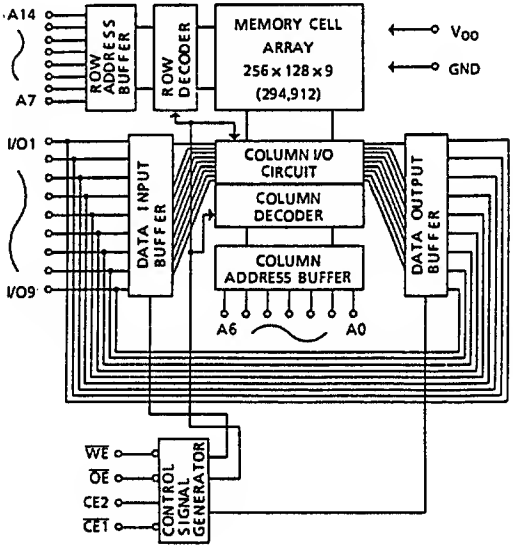
FEATURES

- Fast access time :
  - TC55329P/J-17 17ns(MAX.)
  - TC55329P/J-20 20ns(MAX.)
  - TC55329P/J-25 25ns(MAX.)
  - TC55329P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55329P/J-17 140mA(MAX.)
  - TC55329P/J-20 140mA(MAX.)
  - TC55329P/J-25 140mA(MAX.)
  - TC55329P/J-35 120mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - 32 pin plastic 300 mil DIP : TC55329P
  - 32 pin plastic 300 mil SOJ : TC55329J

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-17	4.75	5.0	5.25	V
		-20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		-0.5 *	-	0.8	V

* -3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			-	-	± 1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0~V_{DD}			-	-	± 1	μA
I_{OOO}	Operating Current	tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	-17	-	-	140	mA
			V_{DD} = 5.5V	-20	-	-	140	
				-25	-	-	140	
				-35	-	-	120	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	-17	-	-	20	mA
			V_{DD} = 5.5V	-20				
				-25				
				-35				
I_{DDS2}		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V Other Input = V_{DD} - 0.2V or 0.2V			-	-	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C(1), -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55329P/J-17		TC55329P/J-20		TC55329P/J-25		TC55329P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	
t_{CO1}	$\overline{CE1}$ Access Time	-	17	-	20	-	25	-	35	
t_{CO2}	CE2 Access Time	-	17	-	20	-	25	-	35	
t_{OE}	$\overline{OE}$ Access Time	-	9	-	10	-	12	-	15	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	-	5	-	5	-	5	-	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	-	10	-	10	-	10	-	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	8	-	8	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	

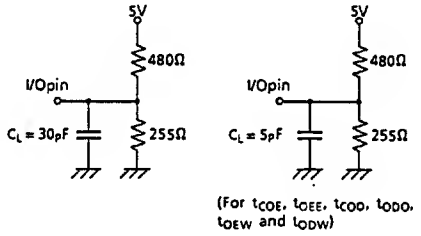
WRITE CYCLE

SYMBOL	PARAMETER	TC55329P/J-17		TC55329P/J-20		TC55329P/J-25		TC55329P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0		
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig.1

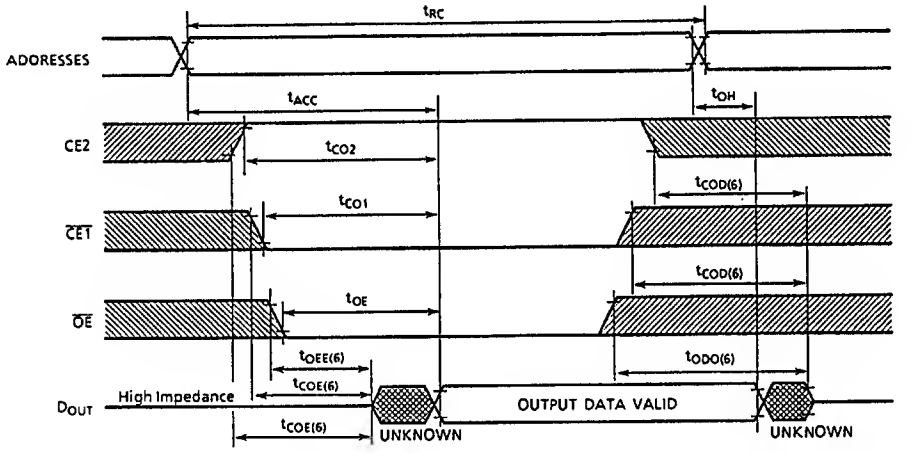
Fig.1



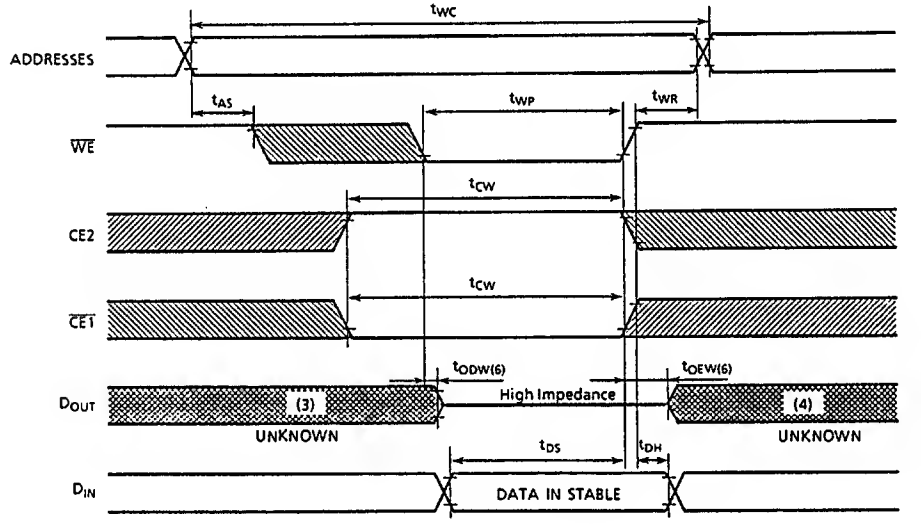
(For t_{COE}, t_{OEE}, t_{COO}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

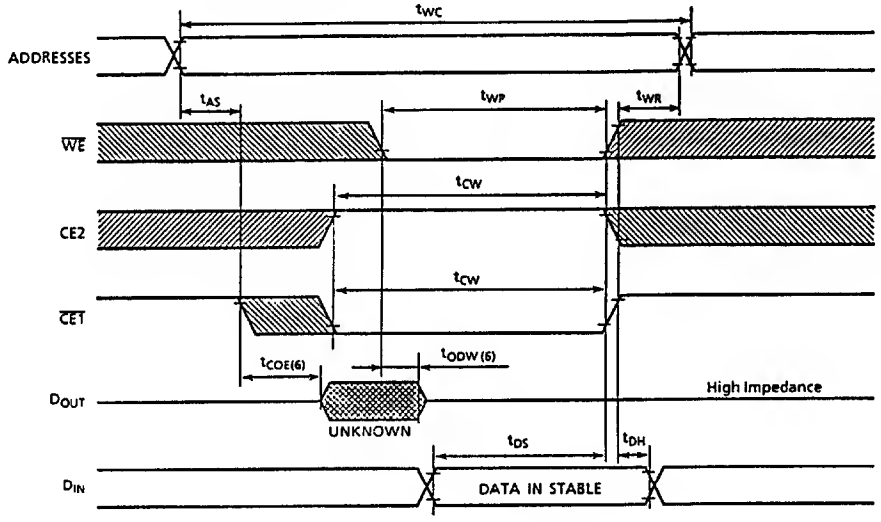
READ CYCLE (2)



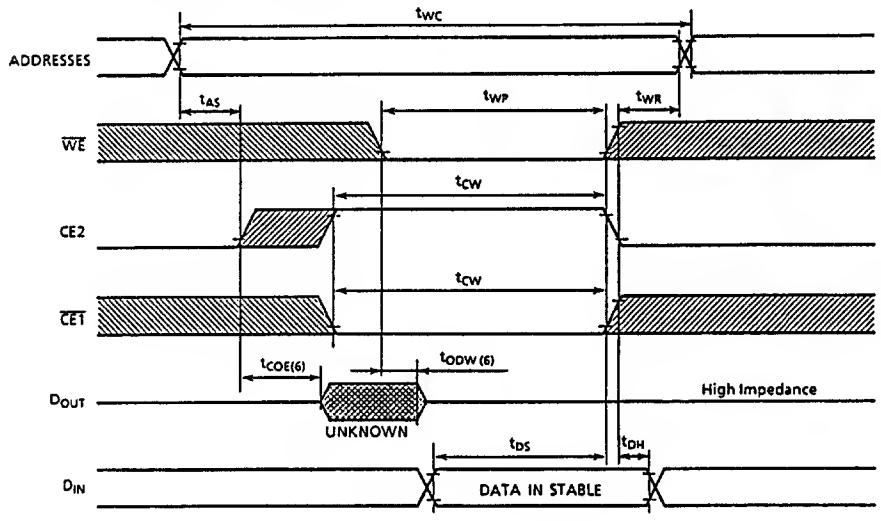
WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

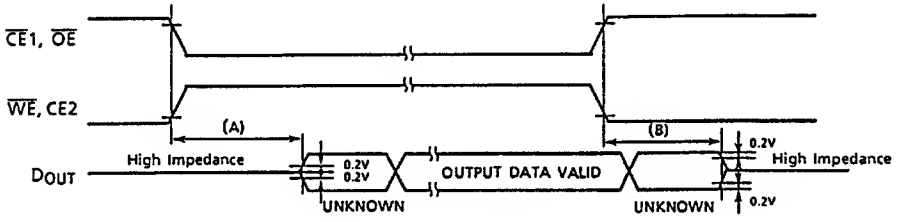
4 Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

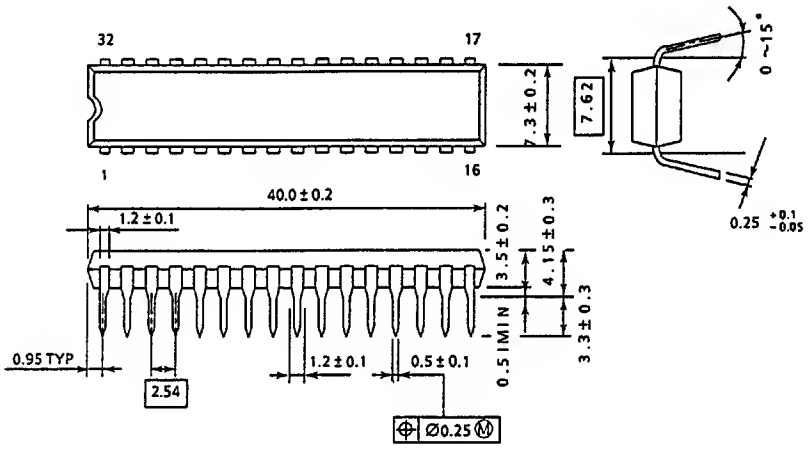
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP32-P-300)

UNIT in mm

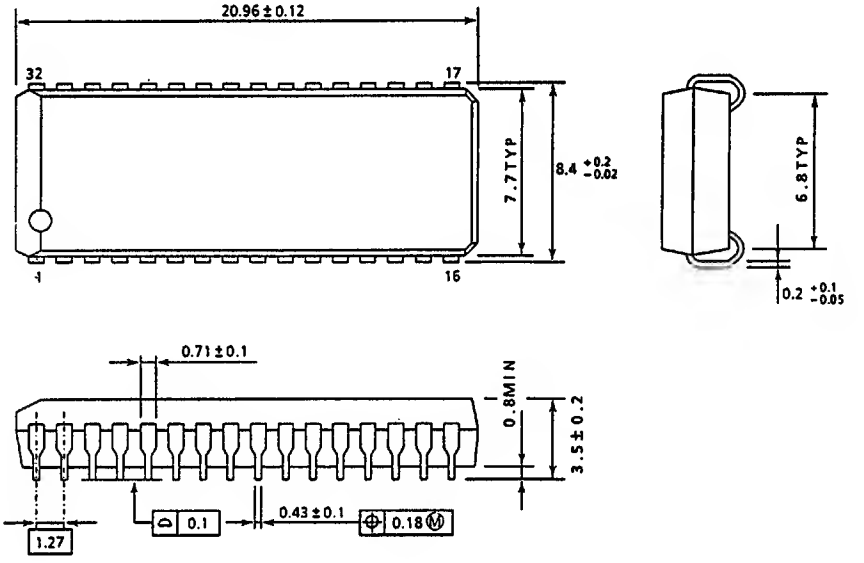


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ32 - P - 300)

UNIT in mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

32,768 WORD × 16 BIT CMOS STATIC RAM **PRELIMINARY**

DESCRIPTION

The TC551632J is a 524,288 bits high speed static random access memory organized as 32,768 words by 16 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551632J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC551632J is suitable for use in various application systems where high speed is required as cache memory. All Inputs and Outputs are directly TTL compatible.

The TC551632J is packaged in a 40 pin plastic SOJ with 400 mil width for high density surface assembly.

FEATURES

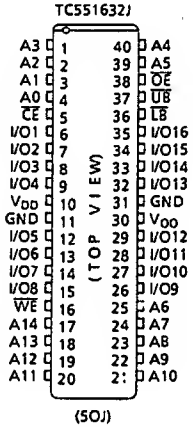
- Fast access time :
  - TC551632J-20 20ns (MAX.)
  - TC551632J-25 25ns (MAX.)
  - TC551632J-35 35ns (MAX.)
- Low power dissipation

Cycle Time	20	25	35	100	ns
Operation (MAX.)	220	200	170	130	mA

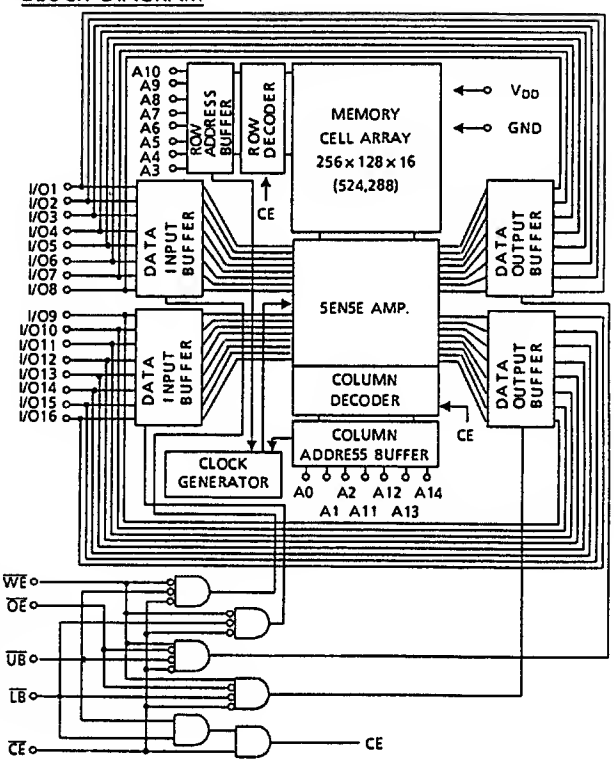
Standby : 1mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Data byte control
  $\overline{LB}$ (I/O1~I/O8), $\overline{UB}$ (I/O9~I/O16)
- Package : SOJ40-P-400

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O16	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
VDD	Power(+ 5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0 * ~7.0	V
$V_{I/O}$	Input / Output Terminal Voltage	-0.5 * ~VDD + 0.5	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

* : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Suply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		-	-	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~VDD		-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH} / V_{IL}	tcycle = 20ns	-	-	220	mA
			tcycle = 25ns	-	-	200	
			tcycle = 35ns	-	-	170	
			tcycle = 100ns	-	-	130	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, or $\overline{UB}$ = $\overline{LB}$ = V_{IH} Other Inputs = V_{IH} / V_{IL}		-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD}−0.2V or $\overline{UB}$ = $\overline{LB}$ = V_{DD}-0.2V Other Inputs = V_{DD}−0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H	High Impedance	High Impedance	I_{DDS}
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	20	–	25	–	35	
t_{CO}	$\overline{CE}$ Access Time	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	10	–	12	–	17	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	20	–	25	–	35	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	1	–	
t_{COO}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	–	8	

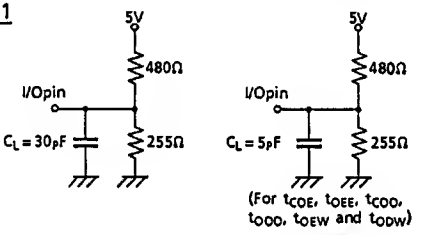
WRITE CYCLE

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	10	–	12	–	16	–	
t_{CW}	Chip Enable to End of Write	13	–	15	–	17	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	13	–	15	–	17	–	
t_{AW}	Address Valid to End of Write	12	–	14	–	16	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{OS}	Data Set Up Time	10	–	10	–	10	–	
t_{DH}	Data Hold Time ($\overline{WE}$)	0	–	0	–	0	–	
t_{DH1}	Data Hold Time ($\overline{CE}$, $\overline{UB}$, $\overline{LB}$)	1	–	1	–	1	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{OOW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC TEST CONDITIONS

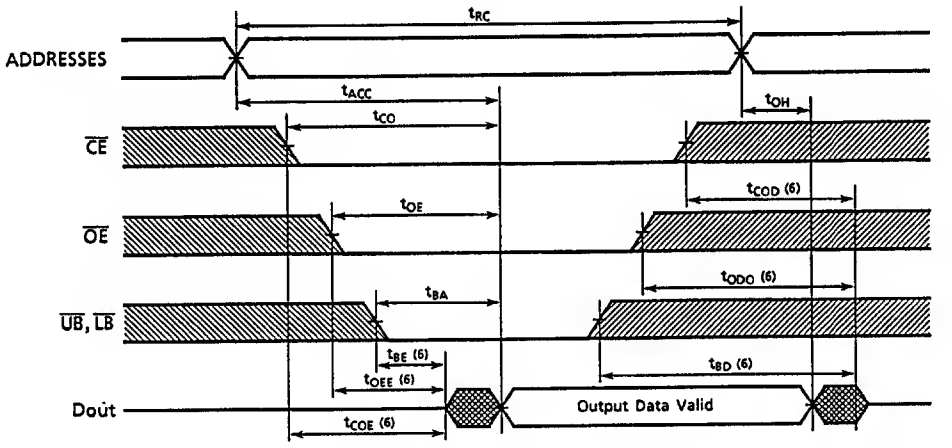
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

FIG. 1

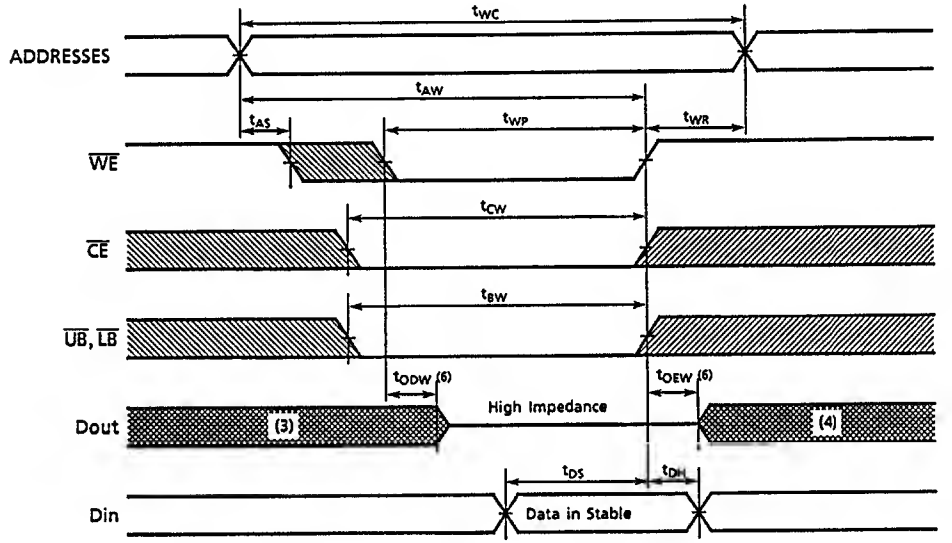


TIMING WAVEFORMS

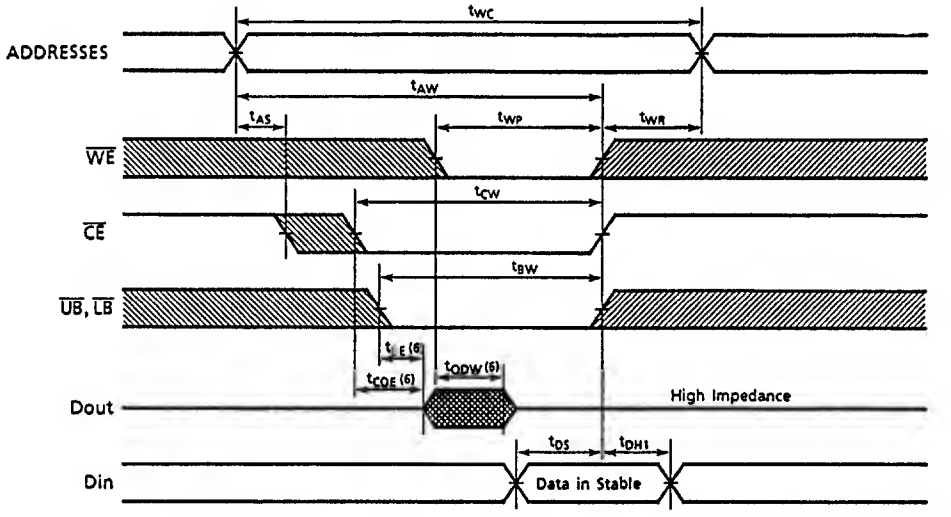
READ CYCLE (2)



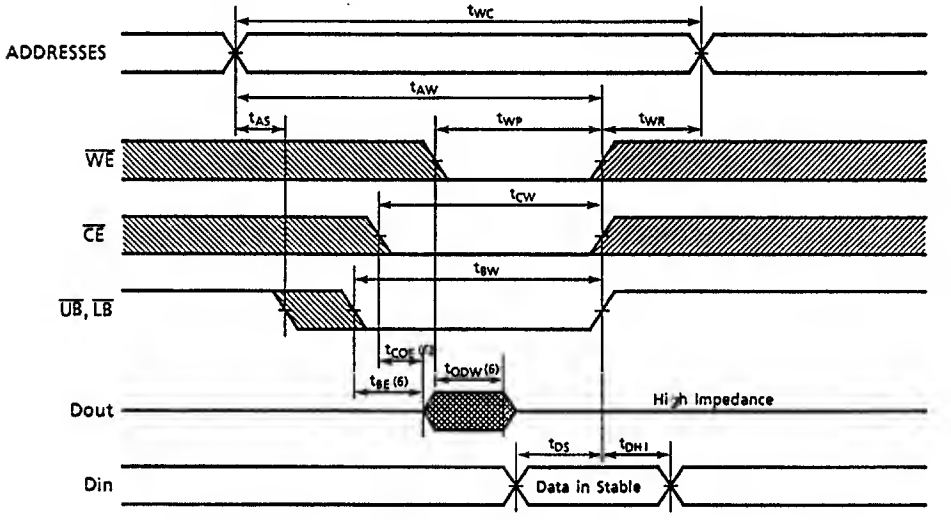
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled)



WRITE CYCLE 3 (5) ($\overline{UB}$, $\overline{LB}$ Controlled)

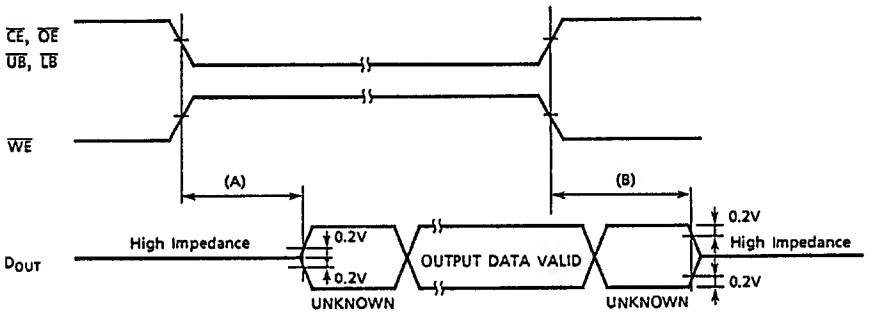


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{WE}$ is High for Read Cycle.
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} ····· Output Enable Time

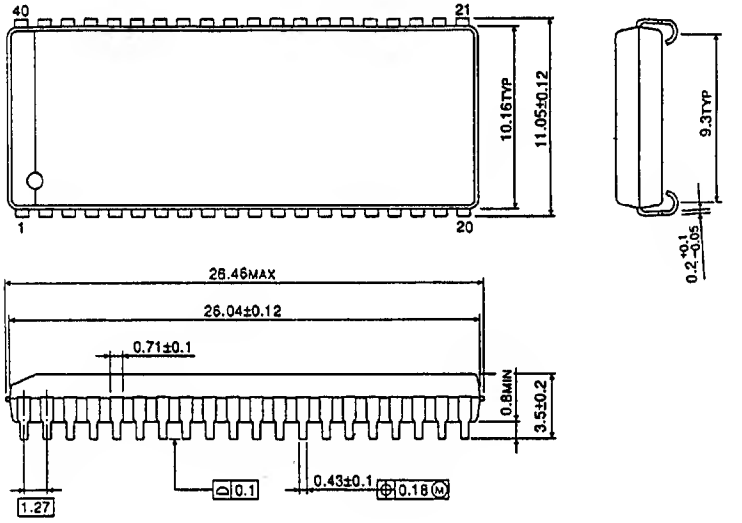
   (B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic SOJ (SOJ40 − P − 400)

UNIT : mm



65,536 WORD × 16 BIT CMOS STATIC RAM

DESCRIPTION

The TC551664J is a 1,048,576 bits high speed static random access memory organized as 65,536 words by 16 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551664J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access. Also it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC551664J is suitable for use in various application systems where high speed is required as cache memory. All Inputs and Outputs are directly TTL compatible.

The TC551664J is packaged in a 44 pin plastic SOJ with 400 mil width for high density surface assembly.

FEATURES

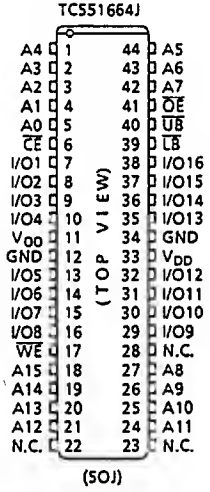
- Fast access time :
  - TC551664J-15 15ns (MAX.)
  - TC551664J-20 20ns (MAX.)
  - TC551664J-25 25ns (MAX.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (MAX.)	260	220	200	180	150	mA

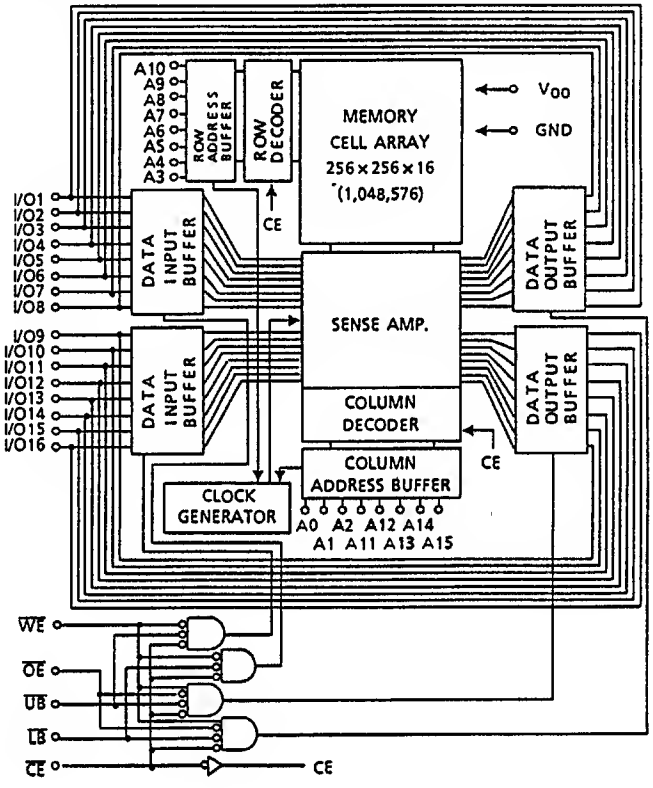
Standby : 1mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Data byte control
  $\overline{LB}$ (I/O1~I/O8), $\overline{UB}$ (I/O9~I/O16)
- Package : SOJ44-P-400

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power(+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0 * ~7.0	V
$V_{I/O}$	Input / Output Terminal Voltage	-0.5 * ~VDD+0.5	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

* : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Suply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5 *	-	0.8	V

* : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		-	-	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~VDD		-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH} / V_{IL}	tcycle = 15ns	-	-	260	mA
			tcycle = 20ns	-	-	220	
			tcycle = 25ns	-	-	200	
			tcycle = 30ns	-	-	180	
			tcycle = 50ns	-	-	150	
I_{OOS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH} / V_{IL}		-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{OO} - 0.2V Other Inputs = V_{OO} - 0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ [1], $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC551664J-15		TC551664J-20		TC551664J-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	20	–	25	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	–	12	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	–	10	–	12	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{OOD}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	–	8	

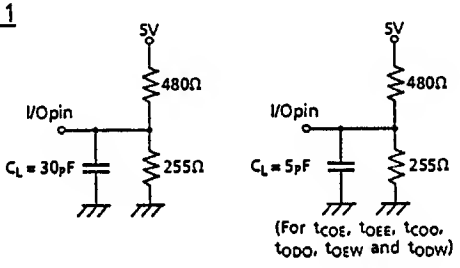
WRITE CYCLE

SYMBOL	PARAMETER	TC551664J-15		TC551664J-20		TC551664J-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	12	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	9	–	12	–	14	–	
t_{AW}	Address Valid to End of Write	9	–	12	–	14	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	8	–	10	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC TEST CONDITIONS

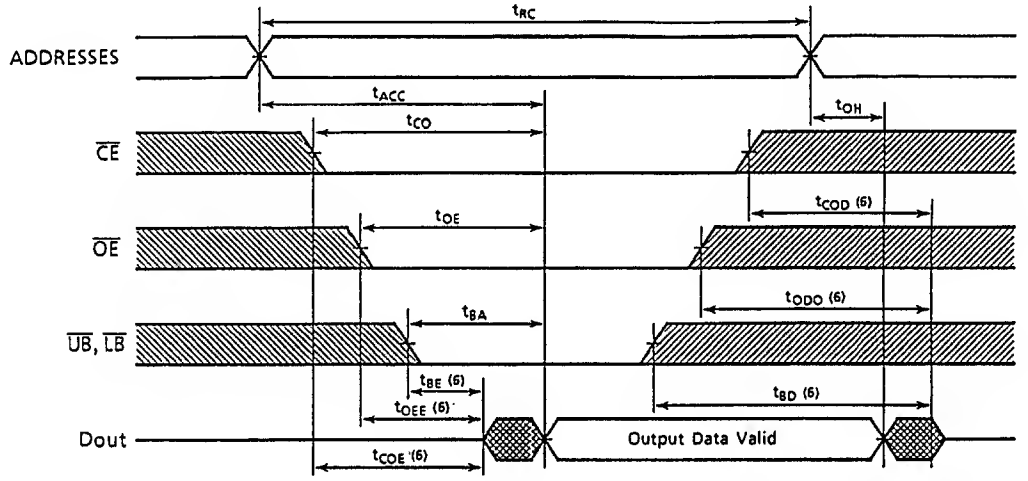
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

FIG. 1

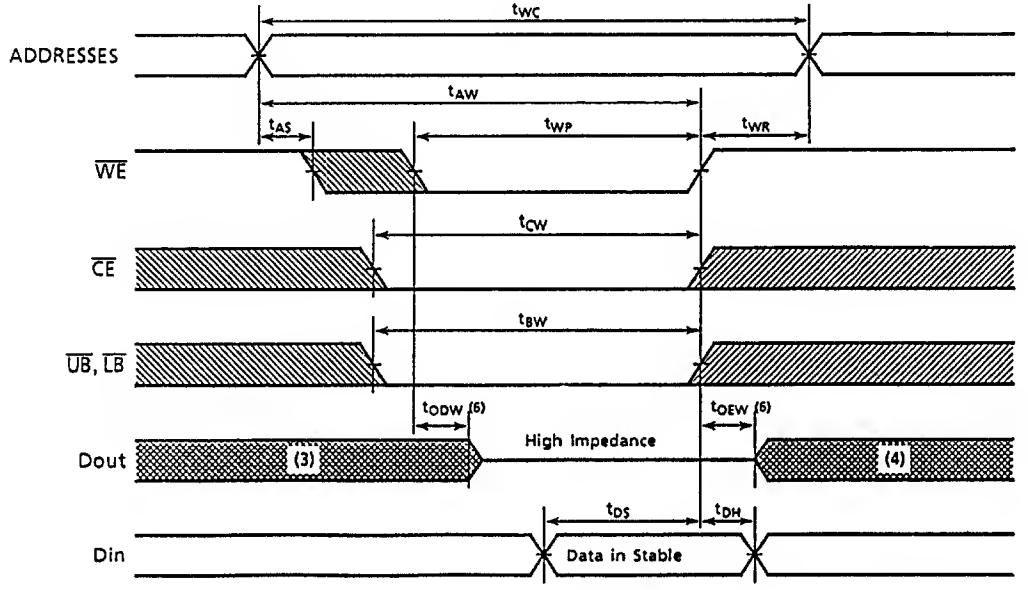


TIMING WAVEFORMS

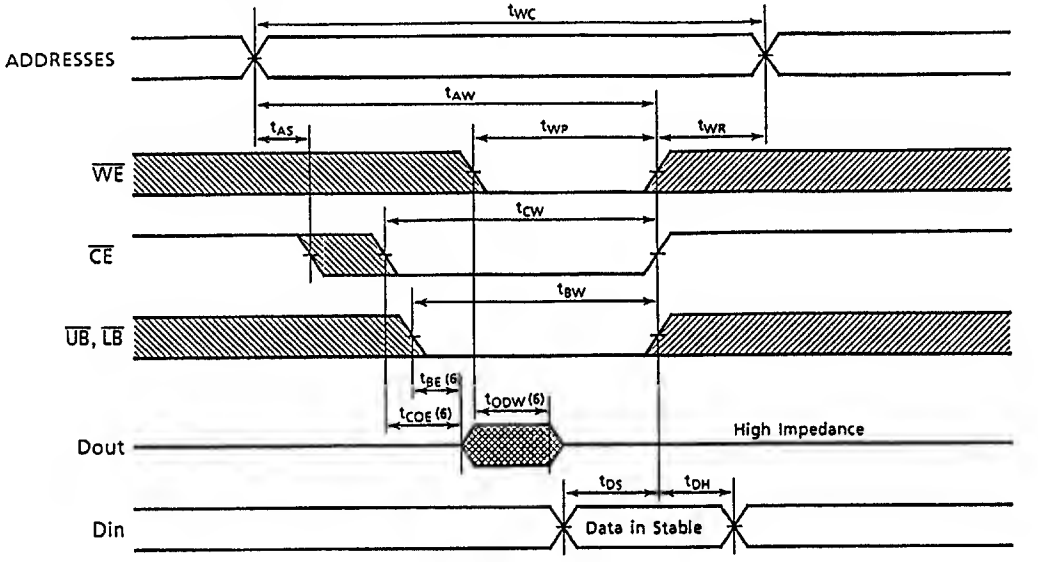
READ CYCLE (2)



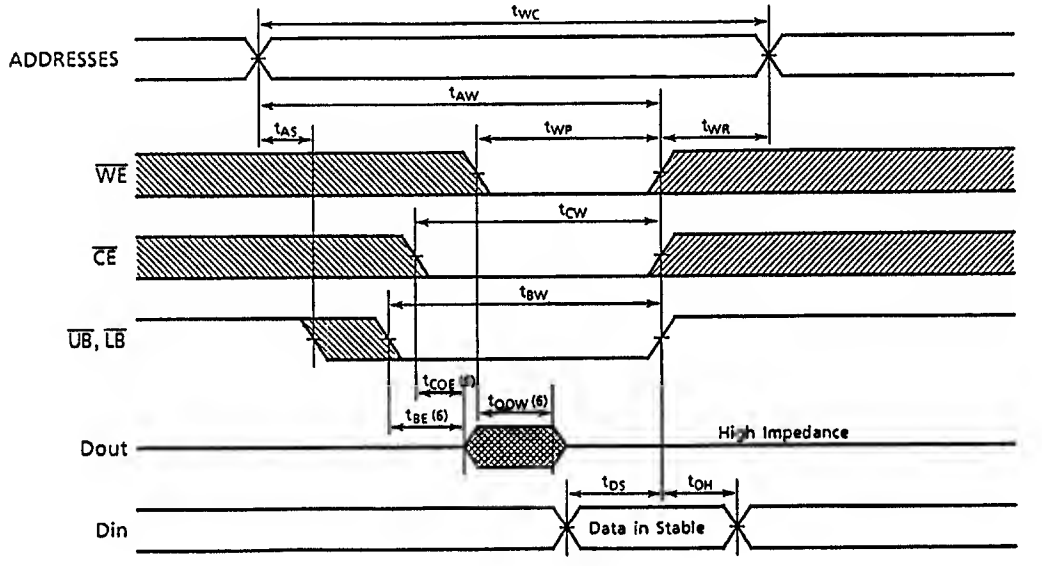
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled)



WRITE CYCLE 3 (5) ($\overline{UB}$, $\overline{LB}$ Controlled)

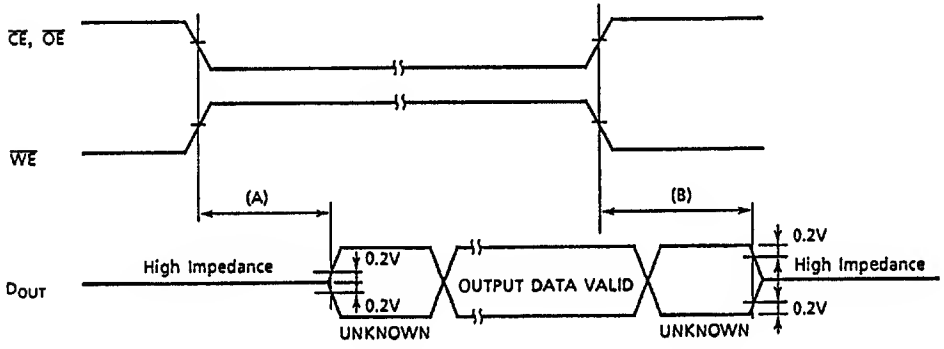


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{WE}$ is High for Read Cycle.
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} ····· Output Enable Time

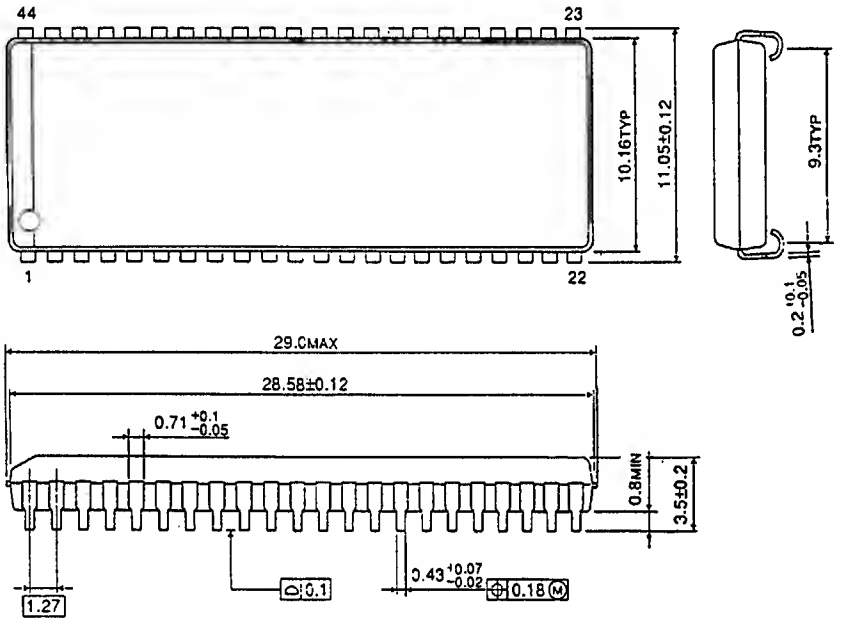
   (B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic SOJ (SOJ44 − P − 400)

UNIT : mm



BiCMOS High Speed Static RAM

8,192 WORD × 8 BIT BiCMOS STATIC RAM

DESCRIPTION

The TC55B88P/J is a 65,536 bits high speed static random access memory organized as 8,192 words by 8 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B88P/J has low power feature with device control using Chip Enable ($\overline{CE1}$/CE2), and has Output Enable Input ($\overline{OE}$) for fast memory access.

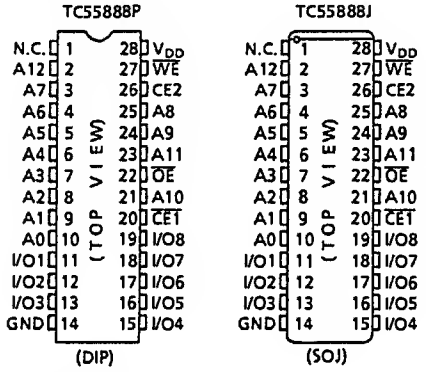
The TC55B88P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B88P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- **Fast access time :**
  - TC55B88P/J-10 10ns (MAX.)
  - TC55B88P/J-12 12ns (MAX.)
- **Low power dissipation :**
  - Operation 155mA (MAX.)
  - Standby 10mA (MAX.)
- **Fully static operation**
- **5V single power supply :**
  - −10 : 5V±5% / −12 : 5V±10%
- **Directly TTL compatible : All Inputs and Outputs**
- **Output buffer control : $\overline{OE}$**
- **Package :**
  - TC55B88P : DIP28-P-300B
  - TC55B88J : SOJ28-P-300A

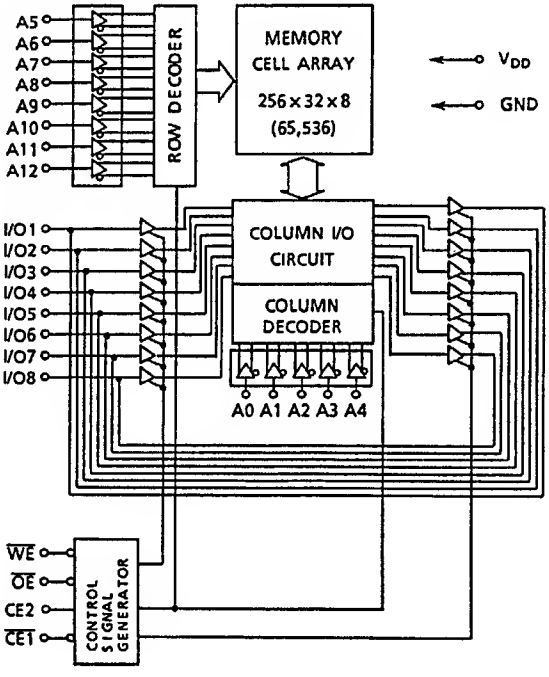
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-10	4.75	5.0	5.25	V
		-12	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		-0.5*	-	0.8	V

* -3V Pulse Width ; 10ns

DC and OPERATING CHARACTERISTICS (Ta=0~70°C, -10 : V_{DD}=5V±5% / -12 : V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±10	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0~V_{DD}			-	-	±10	μA
I_{DDO}	Operating Current	tcycle=Min cycle $\overline{CE1}$=V_{IL} and CE2=V_{IH} Other Inputs=V_{IH}/V_{IL} I_{OUT}=0mA	V_{DD}=5.25V	-10	-	-	155	mA
			V_{DD}=5.5V	-12				
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} Other Inputs=V_{IH}/V_{IL}	V_{DD}=5.25V	-10	-	-	30	mA
			V_{DD}=5.5V	-12				
I_{DDS2}		$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V Other Inputs=V_{DD}-0.2V or 0.2V			-	-	10	

CAPACITANCE (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	7	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (1), −10 : V_{DD} = 5V ± 5% / −12 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55888P/J−10		TC55888P/J−12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	−	12	−	ns
t_{ACC}	Address Access Time	−	10	−	12	
t_{CO1}	$\overline{CE1}$ Access Time	−	10	−	12	
t_{CO2}	CE2 Access Time	−	10	−	12	
t_{OE}	$\overline{OE}$ Access Time	−	6	−	7	
t_{OH}	Output Data Hold Time from Address Change	3	−	3	−	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	3	−	3	−	
t_{COO}	Output Disable Time from $\overline{CE1}$ or CE2	−	5	−	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	−	1	−	
t_{ODO}	Output Disable Time from $\overline{OE}$	−	5	−	6	
t_{PU}	Chip Selection to Power Up Time	0	−	0	−	
t_{PD}	Chip Deselection to Power Down Time	−	10	−	12	

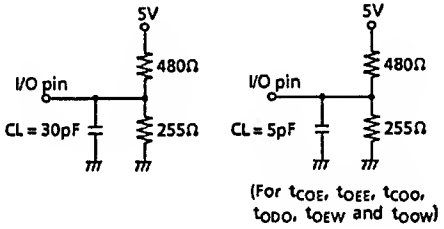
WRITE CYCLE

SYMBOL	PARAMETER	TC55888P/J−10		TC55888P/J−12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	−	12	−	ns
t_{CW}	Chip Enable to End of Write	7	−	8	−	
t_{AS}	Address Set Up Time	0	−	0	−	
t_{AW}	Address Valid to End of Write	7	−	8	−	
t_{WP}	Write Pulse Width	6	−	7	−	
t_{WR}	Write Recovery Time	1	−	1	−	
t_{DS}	Data Set Up Time	6	−	7	−	
t_{DH}	Data Hold Time	0	−	0	−	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	−	1	−	
t_{OOW}	Output Disable Time from $\overline{WE}$	−	5	−	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

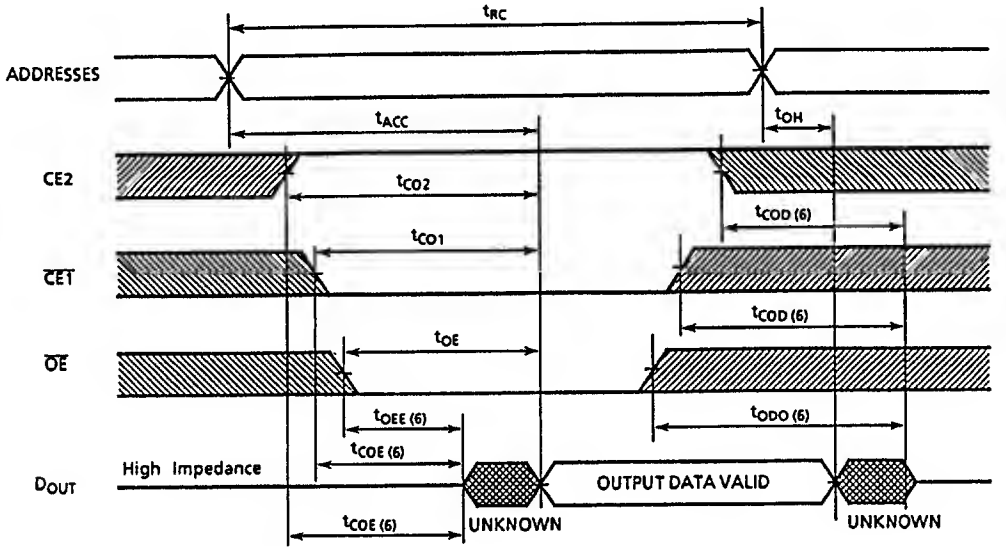
Fig. 1



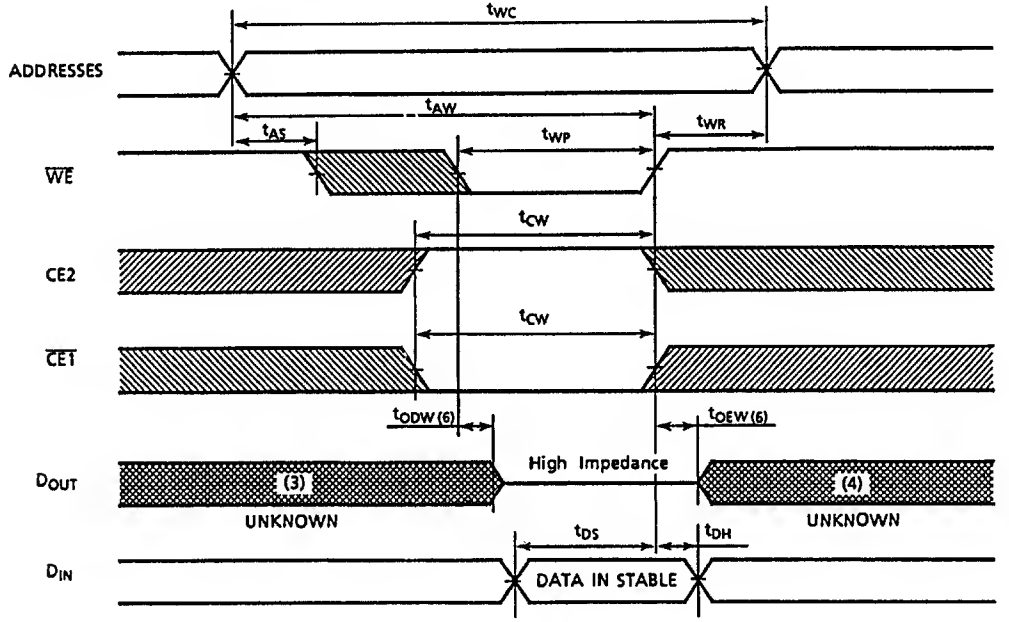
(For t_{COE}, t_{OEE}, t_{COO}, t_{ODO}, t_{OEW} and t_{OOW})

TIMING WAVEFORMS

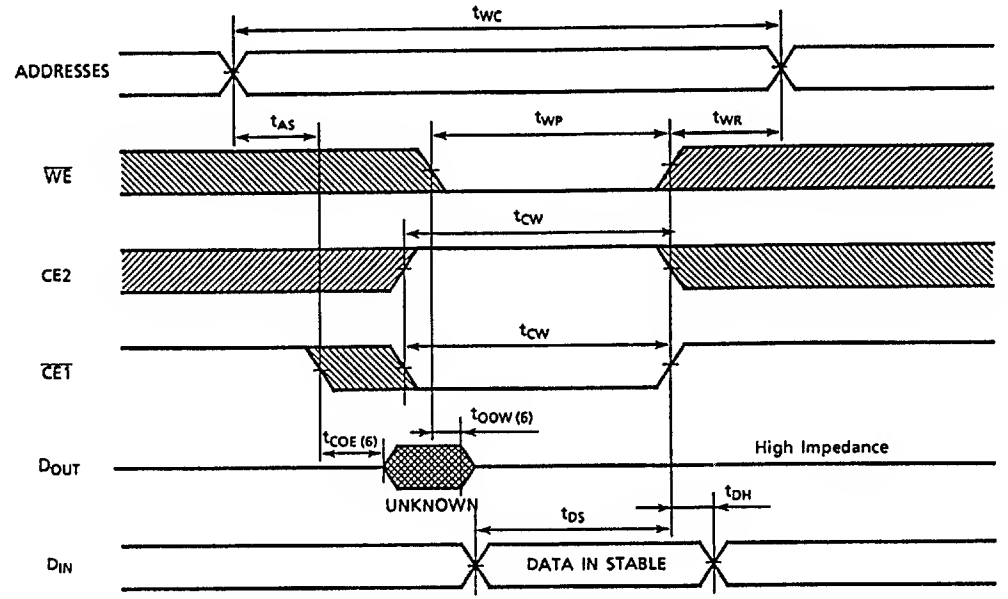
READ CYCLE (2)



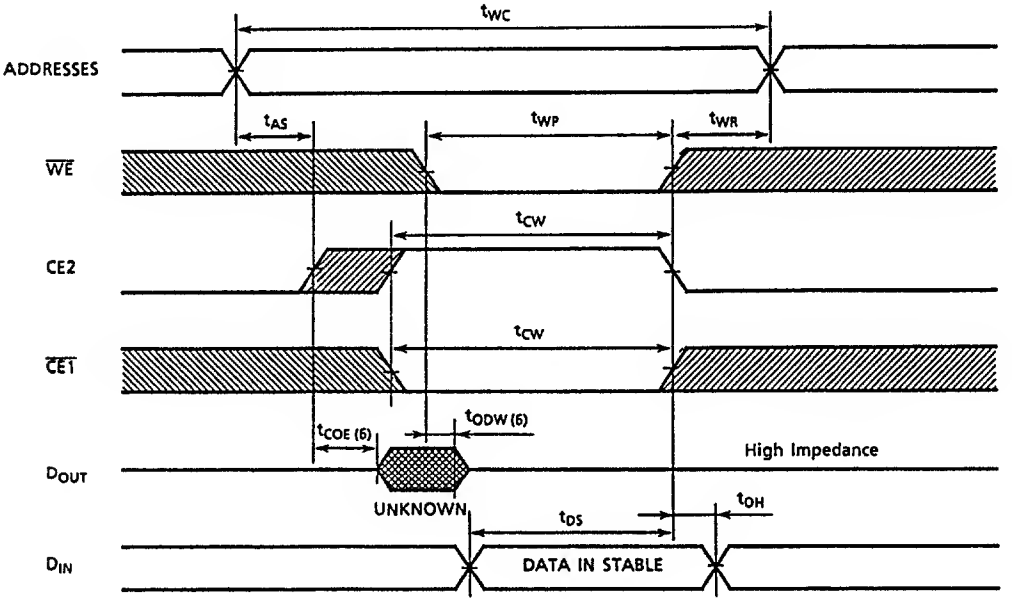
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

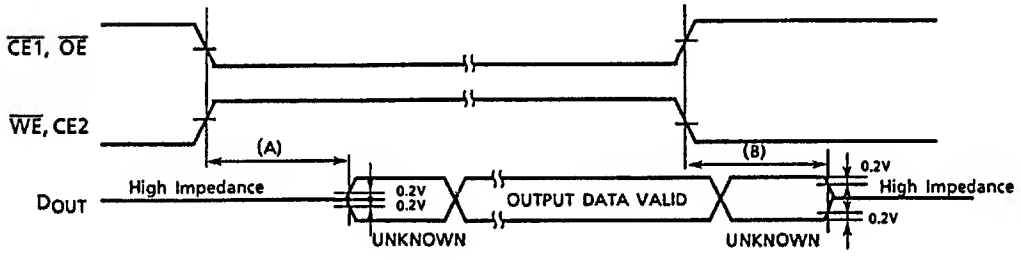
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

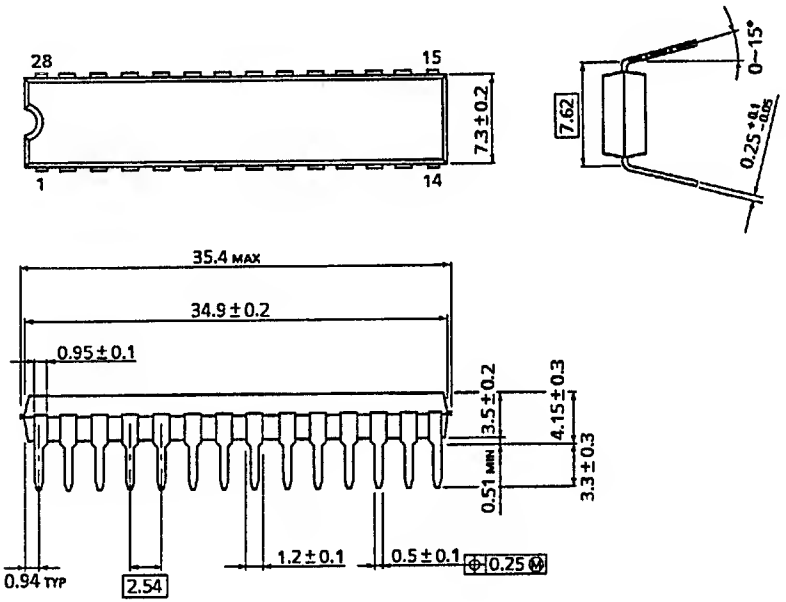
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28−P−300B)

UNIT in mm

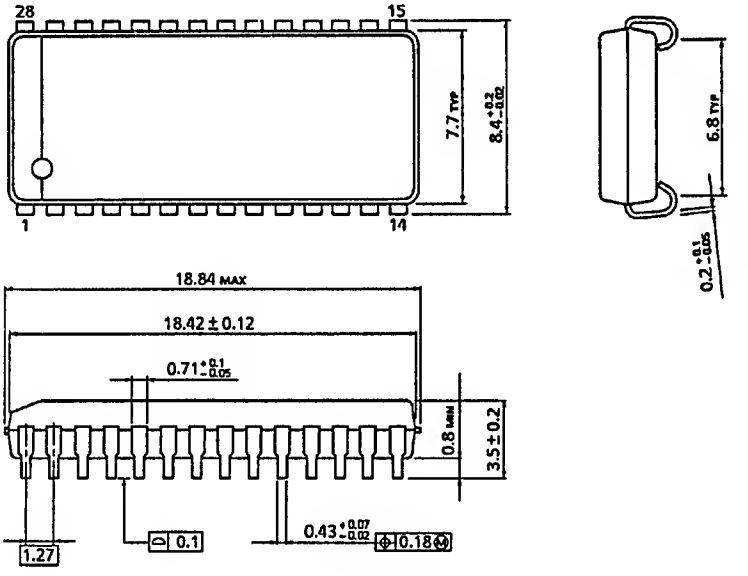


WEIGHT : 2.03g (TYP.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28−P−300A)

UNIT in mm



WEIGHT : 0.83g (TYP.)

16,384 WORD × 4 BIT BiCMOS STATIC RAM

DESCRIPTION

The TC55B417P/J is a 65,536 bits high speed static random access memory organized as 16,384 words by 4 bits using BiCMOS technology, and operated from a single 5 - volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 10ns/12ns and maximum operating current of 120mA at minimum cycle time.

The TC55B417P/J also features an automatic stand - by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 10mA.

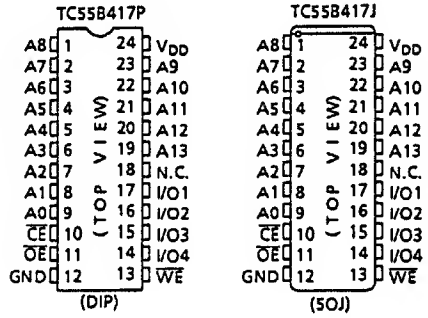
The TC55B417P/J is suitable for use in cache memory where high speed/high density are required.

The TC55B417P/J is packaged in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

FEATURES

- Fast access time:
  - TC55B417P/J-10 — 10ns (MAX.)
  - TC55B417P/J-12 — 12ns (MAX.)
- Low power dissipation:
  - Operation — 120mA (MAX.)
  - Standby — 10mA (MAX.)
- Fully static operation
- 5V single power supply : −10 : 5V±5% / −12 : 5V±10%
- Directly TTL compatible : All Inputs and Outputs
- Output buffer control : $\overline{OE}$
- Package : TC55B417P : DIP24-P-300B
  TC55B417J : SOJ24-P-300A

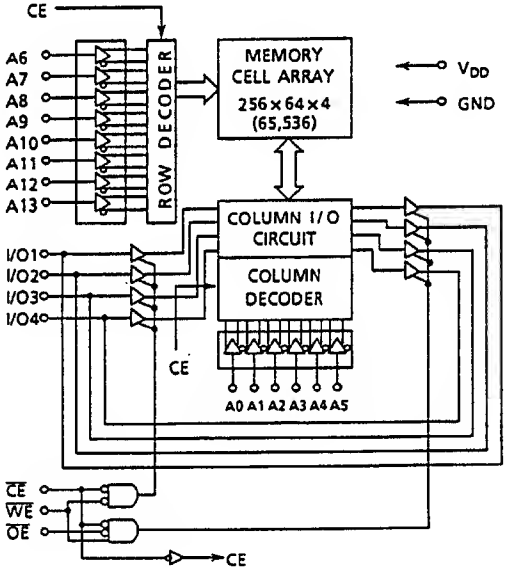
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	850	mW
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	-10	4.75	5.0	5.25	V
		-12	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		-0.5*	-	0.8	V

* -3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta=0~70°C, -10 : V_{DD}=5V±5% / -12 : V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±10	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0~V_{DD}			-	-	±10	μA
I_{DDO}	Operating Current	tcycle=Min cycle, $\overline{CE}$=V_{IL} Iout=0mA Other Inputs=V_{IH}/V_{IL}	V_{DD}=5.25V	-10	-	-	120	mA
			V_{DD}=5.5V	-12				
I_{DDS1}	Standby Current	$\overline{CE}$=V_{IH} Other Inputs=V_{IH}/V_{IL}	V_{DD}=5.25V	-10	-	-	30	mA
			V_{DD}=5.5V	-12				
I_{DDS2}		$\overline{CE}$=V_{DD}-0.2V Other Inputs=V_{DD}-0.2V or 0.2V			-	-	10	

CAPACITANCE (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	7	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (4), -10 : V_{DD} = 5V ± 5% / -12 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	-	12	-	ns
t_{ACC}	Address Access Time	-	10	-	12	
t_{CO}	Chip Enable Access Time	-	10	-	12	
t_{OE}	Output Enable Access Time	-	6	-	7	
t_{COE}	Output Enable Time from $\overline{CE}$	3	-	3	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	5	-	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	-	1	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	5	-	6	
t_{OH}	Output Data Hold Time from Address Change	3	-	3	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	
t_{PO}	Chip Deselection to Power Down Time	-	10	-	12	

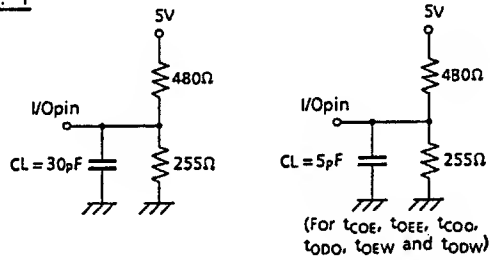
WRITE CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	-	12	-	ns
t_{WP}	Write Pulse Width	6	-	7	-	
t_{AW}	Address Valid to End of Write	7	-	8	-	
t_{CW}	Chip Enable to End of Write	7	-	8	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	5	-	6	
t_{DS}	Data Set Up Time	6	-	7	-	
t_{OH}	Data Hold Time	0	-	0	-	

AC TEST CONDITIONS

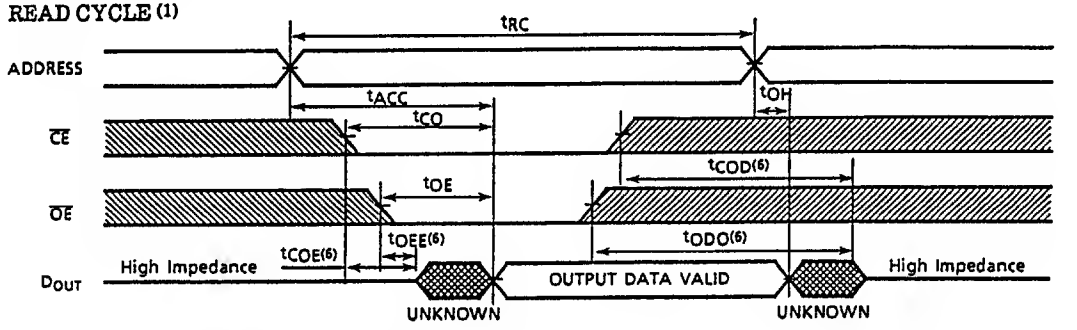
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

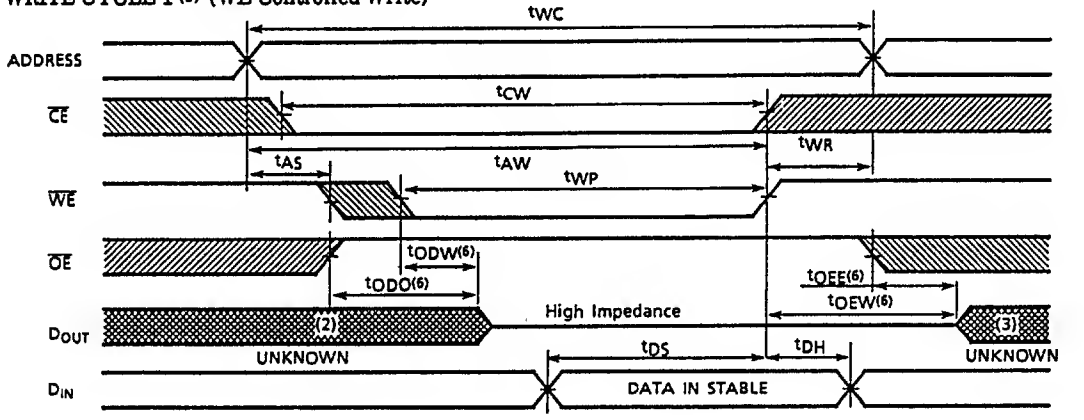


TIMING WAVEFORMS

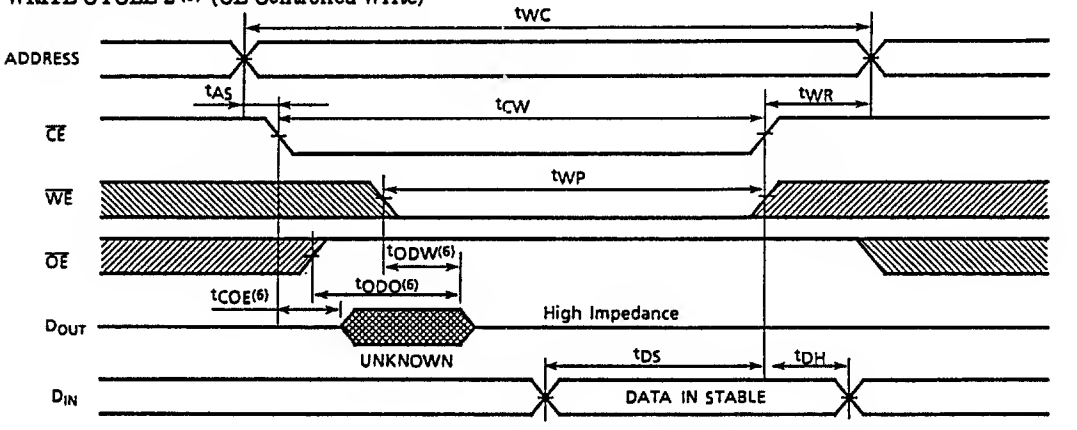
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

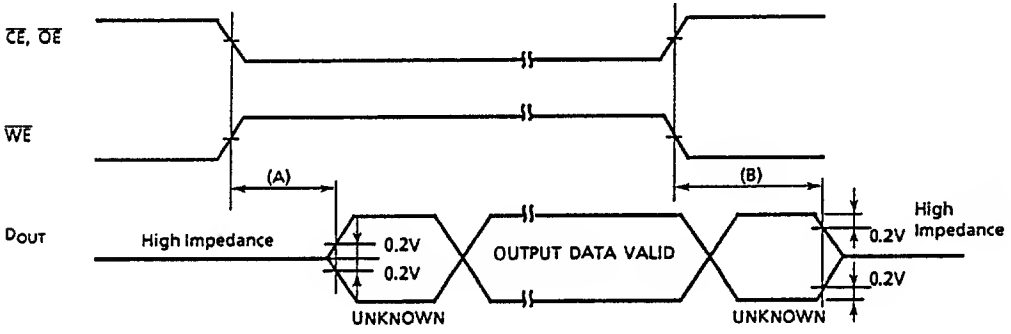
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

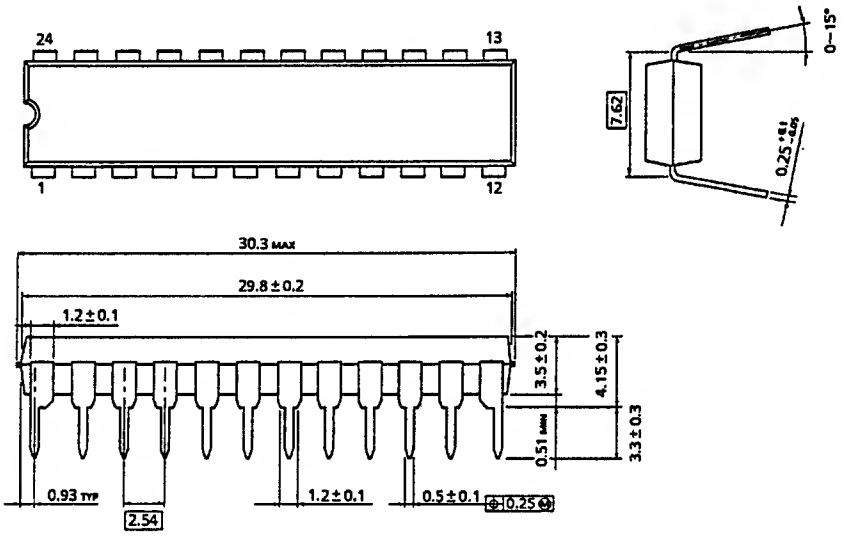
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24−P−300B)

Unit in mm

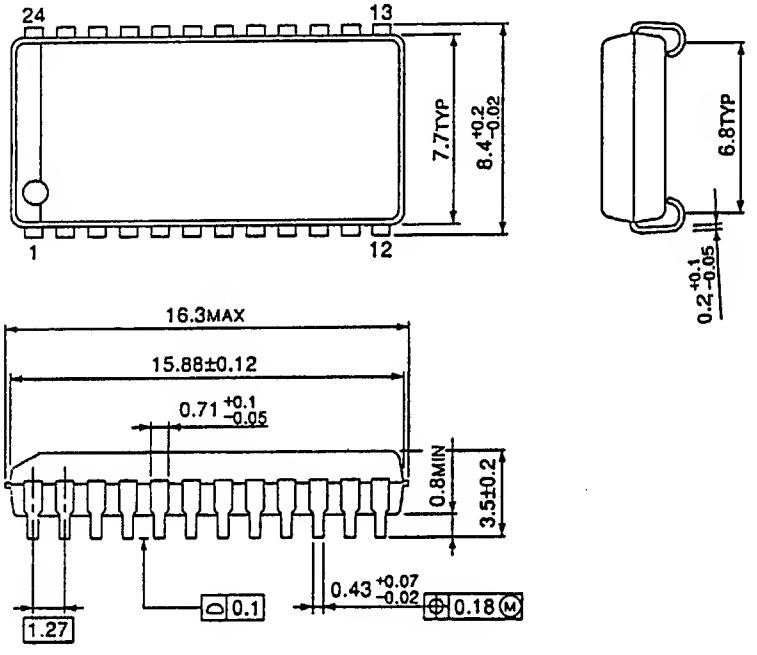


Weight : 1.72g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ24−P−300A)

Unit in mm



Weight : 0.72g (Typ.)

65,536 WORD × 4 BIT Bi CMOS STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55B464P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B464P/J has low power feature with device control using Chip Enable ($\overline{CE}$).

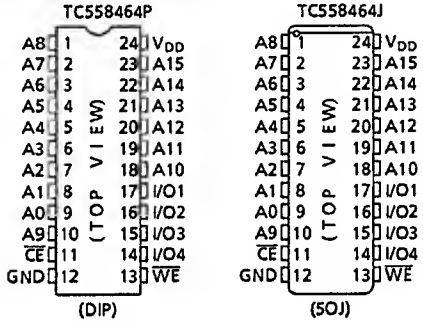
The TC55B464P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B464P/J is packaged in a 24 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B464P/J-10 10ns(MAX.)
  - TC55B464P/J-12 12ns(MAX.)
  - TC55B464P/J-15 15ns(MAX.)
- Low power dissipation
  - Operation : TC55B464P/J-10 140mA(MAX.)
  - TC55B464P/J-12 140mA(MAX.)
  - TC55B464P/J-15 140mA(MAX.)
  - Standby : 15mA(MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package TC55B464P : DIP24-P-300B
  TC55B464J : SOJ24-P-300A

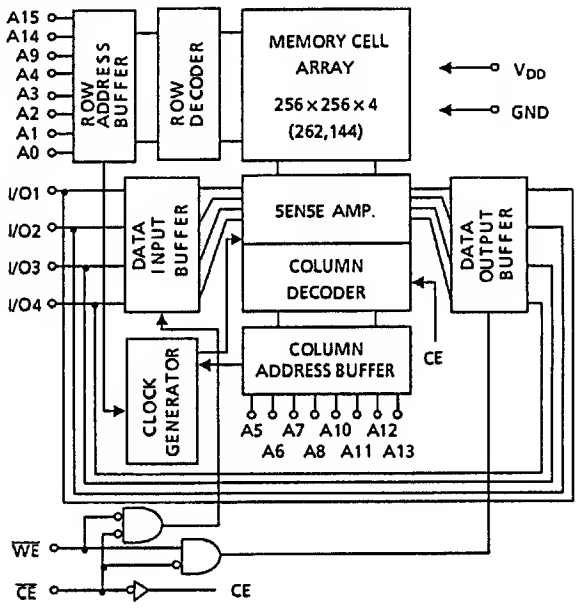
PIN CONNECTION



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power(+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

* : -3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : -3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, I_{OUT} = 0mA	-	-	140	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	15	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATION MODE	$\overline{CE}$	$\overline{WE}$	I/O1~I/O4	POWER
Read	L	H	Output	I_{DDO}
Write	L	L	Input	I_{DDO}
Standby	H	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C (1), V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		TC55B464P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	15	–	ns
t_{ACC}	Address Access Time	–	10	–	12	–	15	ns
t_{CO}	$\overline{CE}$ Access Time	–	10	–	12	–	15	ns
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	3	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	3	–	3	–	3	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	5	–	6	–	6	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	–	15	ns

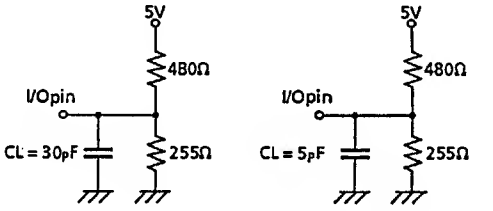
WRITE CYCLE

SYMBOL	PARAMETER	TC55B464P/J-10		TC55B464P/J-12		TC55B464P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	15	–	ns
t_{CW}	Chip Enable to End of Write	7	–	8	–	9	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	ns
t_{AW}	Address Valid to end of write	7	–	8	–	9	–	ns
t_{WP}	Write Pulse Width	6	–	7	–	8	–	ns
t_{WR}	Write Recovery Time	1	–	1	–	1	–	ns
t_{DS}	Data Set Up Time	6	–	7	–	8	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	5	–	6	–	6	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Ref – erence Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

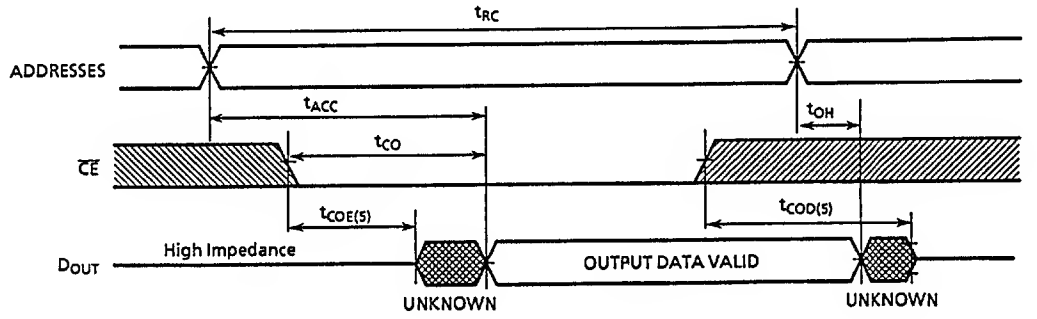
Fig. 1



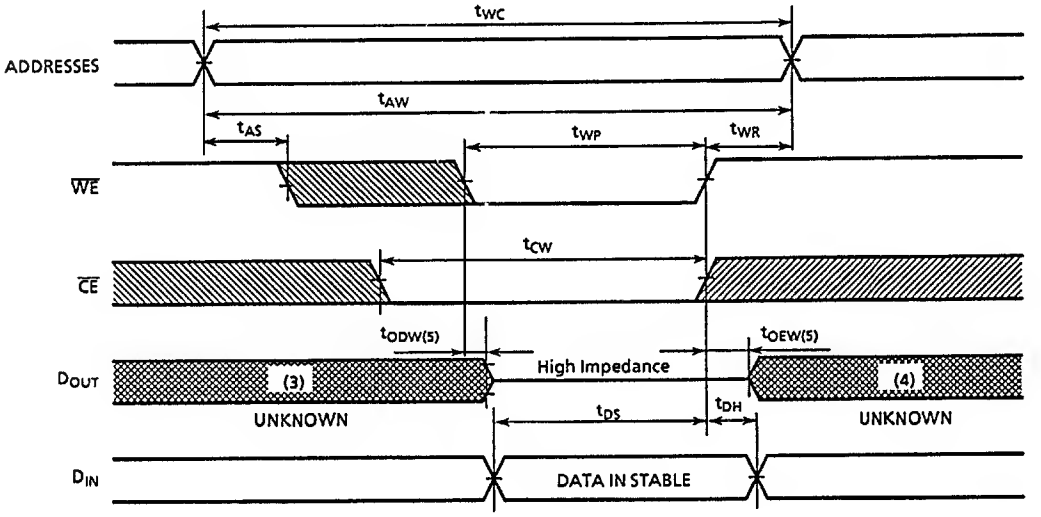
(For t_{COE}, t_{COD}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

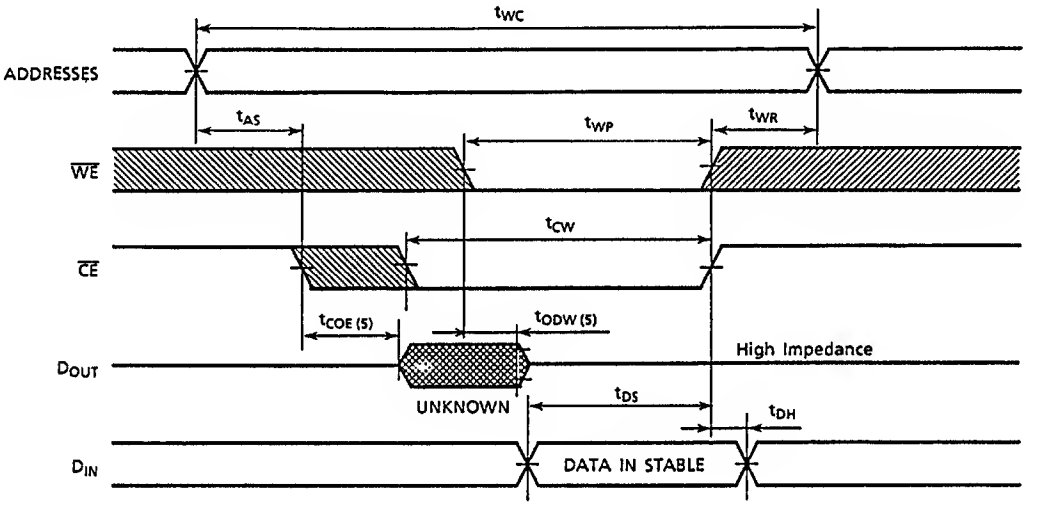
READ CYCLE (2)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



Note: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

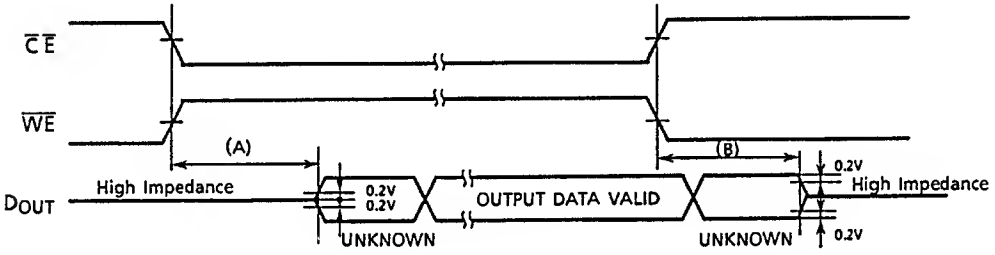
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEW} ····· Output Enable Time

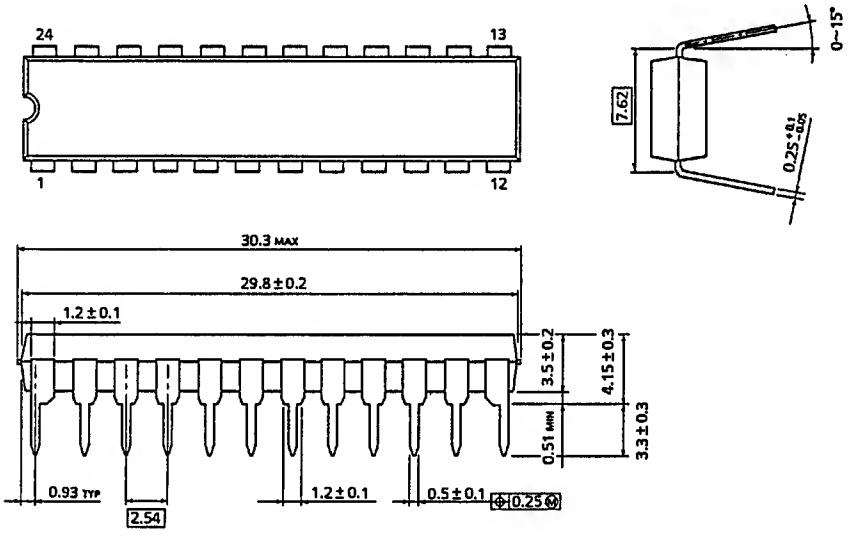
   (B) t_{COD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24 - P - 300B)

UNIT in mm

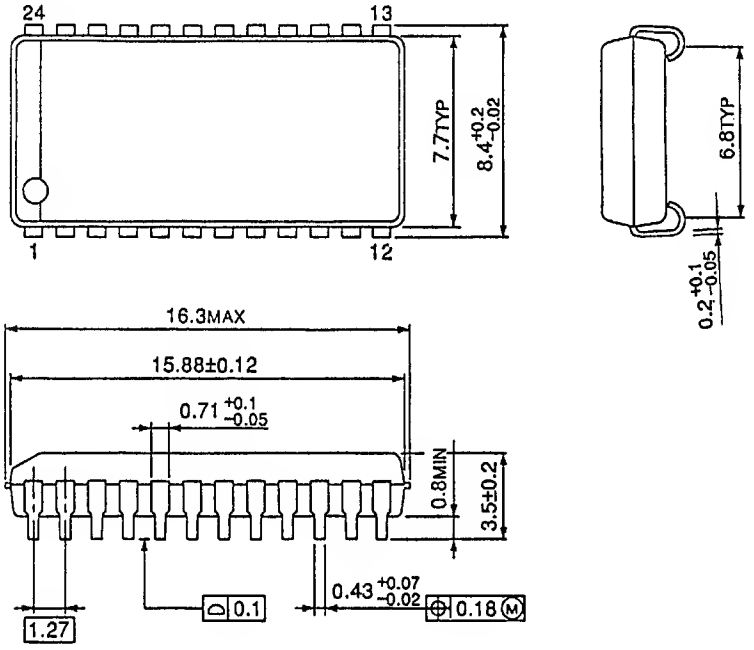


Weight : 1.72g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ24−P−300A)

UNIT in mm



Weight : 0.72g (Typ.)

65,536 WORD × 4 BIT BiCMOS STATIC RAM PRELIMINARY

DESCRIPTION

The TC55B465P/J is a 262,144 bits high speed static random access memory organized as 65,536 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B465P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access.

The TC55B465P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B465P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time:

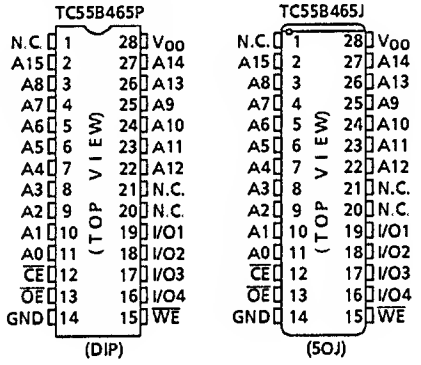
	TC55B465P/J-10	10ns (MAX.)
	TC55B465P/J-12	12ns (MAX.)
	TC55B465P/J-15	15ns (MAX.)

- Low power dissipation

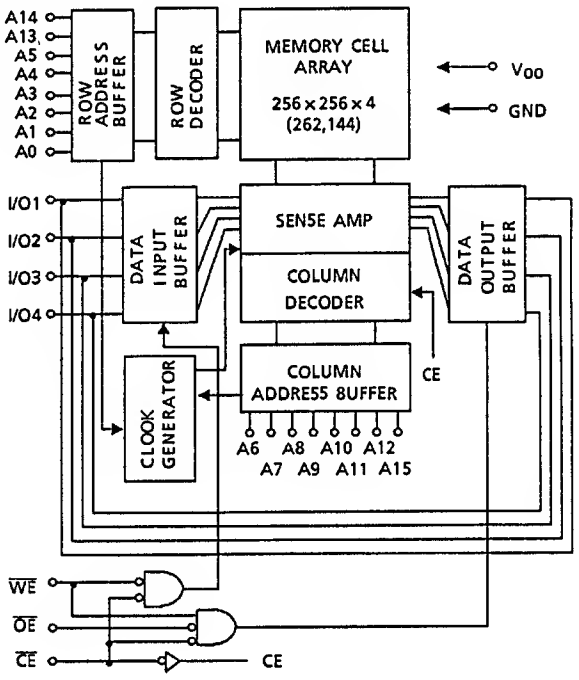
Operation :	TC55B465P/J-10	140mA (MAX.)
	TC55B465P/J-12	140mA (MAX.)
	TC55B465P/J-15	140mA (MAX.)
Standby :		15mA (MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55B465P : DIP28-P-300B
  - TC55B465J : SOJ28-P-300A

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/01~I/04	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

*: -3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

*: -3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, I_{OUT} = 0mA	-	-	140	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	15	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1~I/O4	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C(1), V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		TC55B465P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	-	12	-	15	-	ns
t_{ACC}	Address Access Time	-	10	-	12	-	15	ns
t_{CO}	$\overline{CE}$ Access Time	-	10	-	12	-	15	ns
t_{OE}	$\overline{OE}$ Access Time	-	5	-	6	-	8	ns
t_{OH}	Output Data Hold Time from Address Change	3	-	3	-	3	-	ns
t_{COE}	Output Enable Time from $\overline{CE}$	3	-	3	-	3	-	ns
t_{COO}	Output Disable Time from $\overline{CE}$	-	5	-	6	-	6	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	1	-	1	-	1	-	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	-	5	-	6	-	6	ns
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	ns
t_{PD}	Chip Deselection to Power Down Time	-	10	-	12	-	15	ns

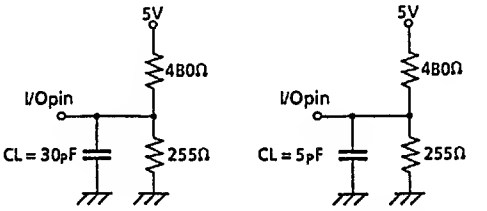
WRITE CYCLE

SYMBOL	PARAMETER	TC55B465P/J-10		TC55B465P/J-12		TC55B465P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	-	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	7	-	8	-	9	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	0	-	ns
t_{AW}	Address Valid to end of write	7	-	8	-	9	-	ns
t_{WP}	Write Pulse Width	6	-	7	-	8	-	ns
t_{WR}	Write Recovery Time	1	-	1	-	1	-	ns
t_{DS}	Data Set Up Time	6	-	7	-	8	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	-	5	-	6	-	6	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Ref-erence Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

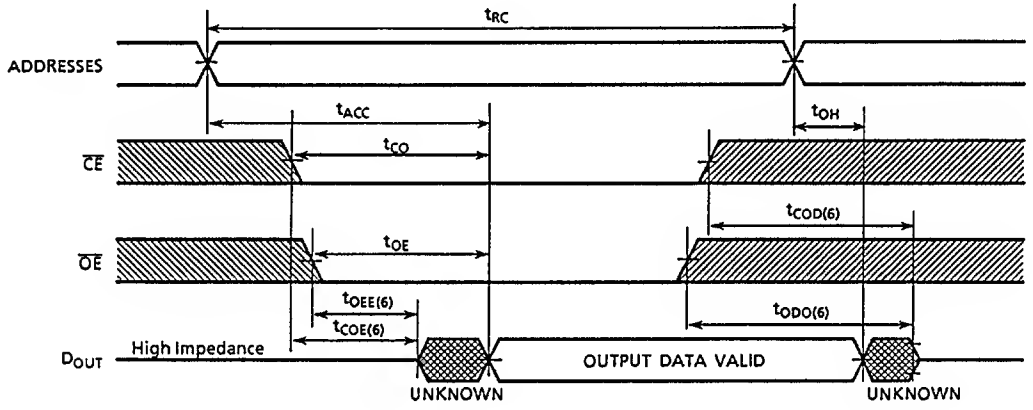
Fig. 1



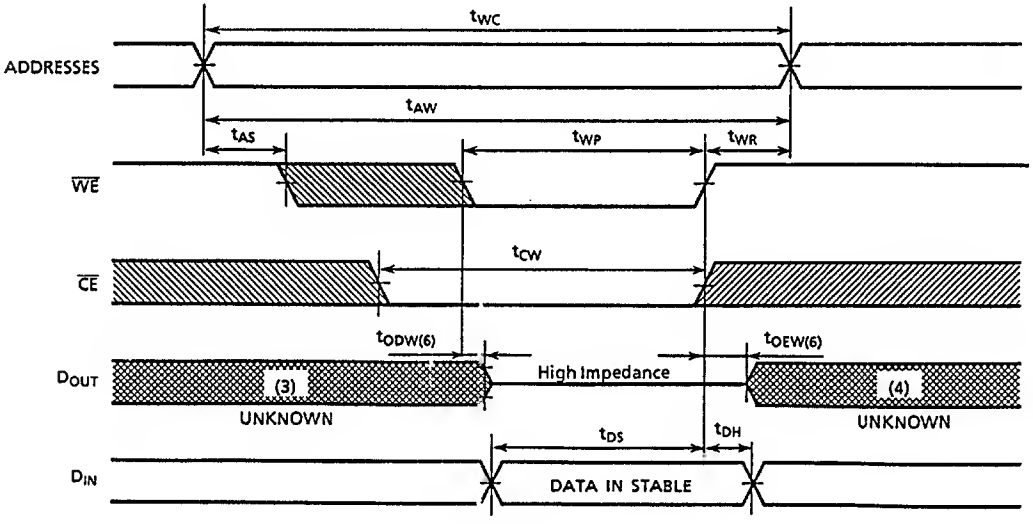
(For t_{COE}, t_{OEE}, t_{COO}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

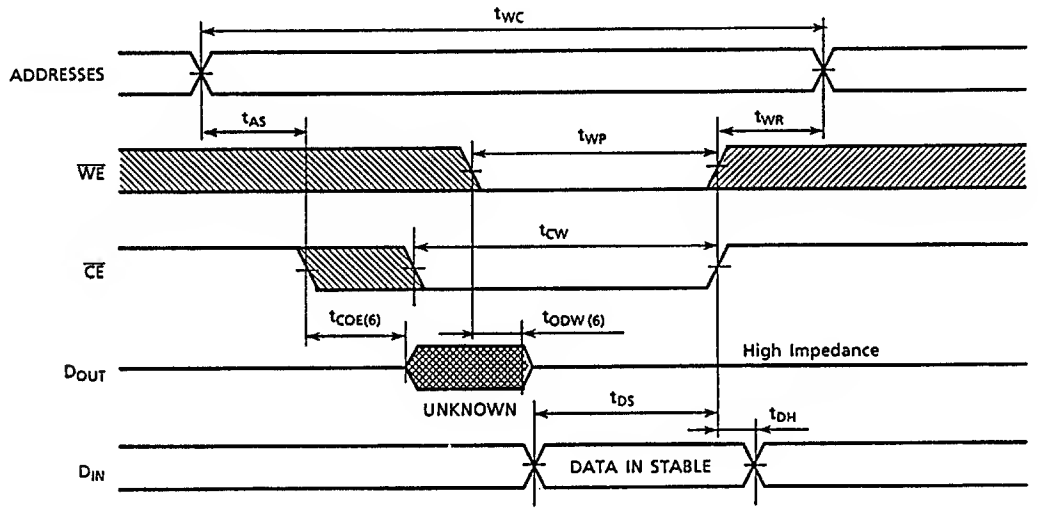
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

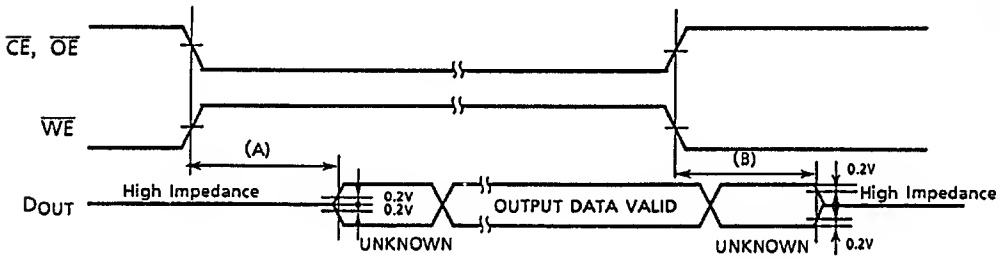
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

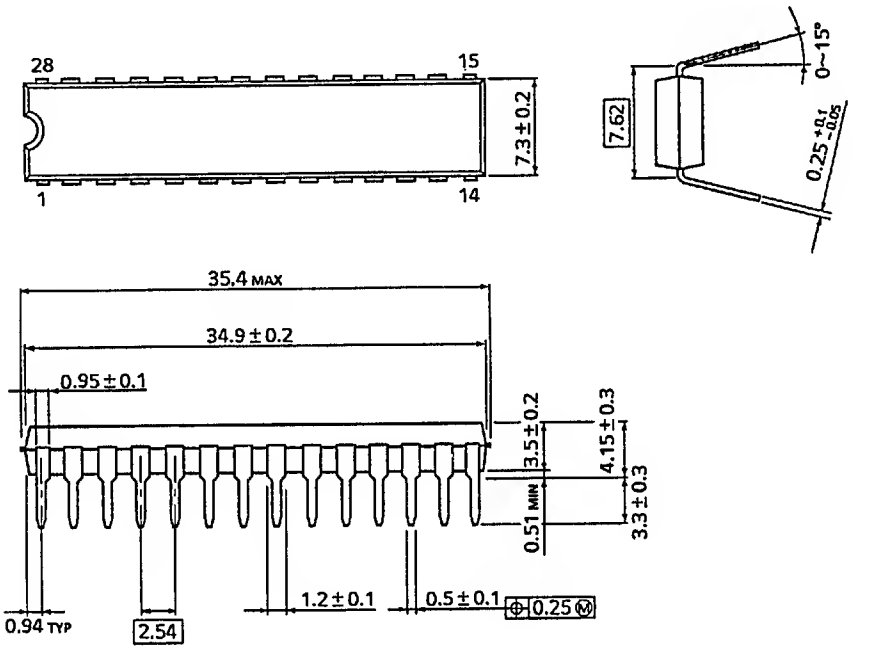
   (B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28 − P − 300B)

Unit in mm

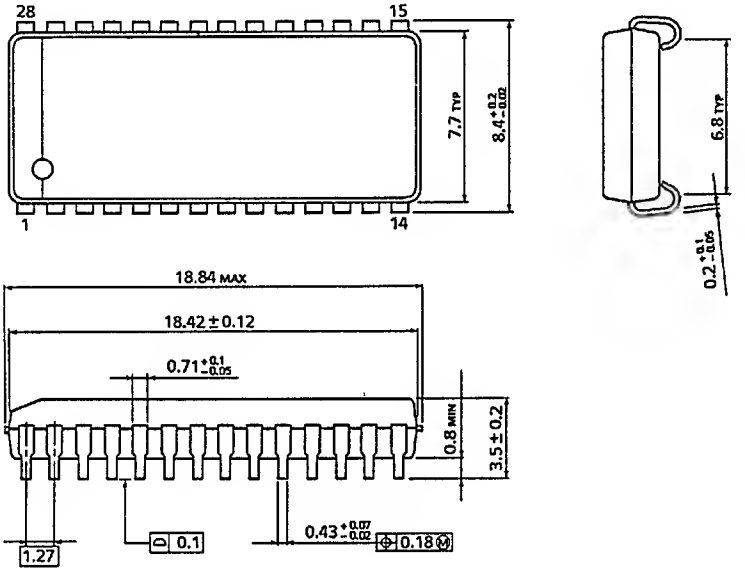


WEIGHT : 2.03g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28 – P – 300A)

UNIT in mm



WEIGHT : 0.83g (Typ.)

32,768 WORD × 8 BIT BiCMOS STATIC RAM **PRELIMINARY**

DESCRIPTION

The TC55B328P/J is a 262,144 bits high speed static random access memory organized as 32,768 words by 8 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provide high speed feature.

The TC55B328P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access.

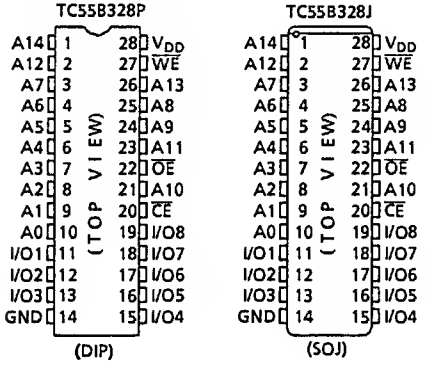
The TC55B328P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B328P/J is packaged in a 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time:
  - TC55B328P/J-10 10ns (MAX.)
  - TC55B328P/J-12 12ns (MAX.)
  - TC55B328P/J-15 15ns (MAX.)
- Low power dissipation
  - Operation: TC55B328P/J-10 170mA (MAX.)
  - TC55B328P/J-12 170mA (MAX.)
  - TC55B328P/J-15 170mA (MAX.)
  - Standby: 15mA (MAX.)
- 5V single power supply: 5V±10%
- Fully static operation
- All Inputs and Outputs: TTL compatible
- Output buffer control: $\overline{OE}$
- Package
  - TC55B328P: DIP28-P-300B
  - TC55B328J: SOJ28-P-300A

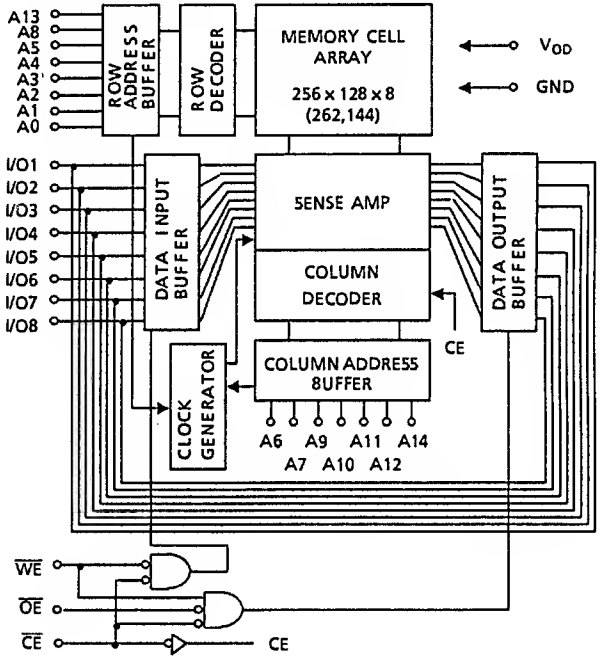
PIN CONNECTION



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

*: −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5*	−	0.8	V

*: −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	−	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	−	−	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	−	−	mA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, Iout = 0mA	−	−	170	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}	−	−	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V	−	−	15	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1~I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C (1), V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B32BP/J-10		TC55B32BP/J-12		TC55B32BP/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	-	12	-	15	-	ns
t_{ACC}	Address Access Time	-	10	-	12	-	15	
t_{CO}	$\overline{CE}$ Access Time	-	10	-	12	-	15	
t_{OE}	$\overline{OE}$ Access Time	-	5	-	6	-	8	
t_{OH}	Output Data Hold Time from Address Change	3	-	3	-	3	-	
t_{COE}	Output Enable Time from $\overline{CE}$	3	-	3	-	3	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	5	-	6	-	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	-	1	-	1	-	
t_{OOO}	Output Disable Time from $\overline{OE}$	-	5	-	6	-	6	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	10	-	12	-	15	

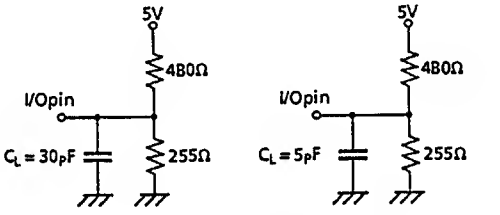
WRITE CYCLE

SYMBOL	PARAMETER	TC55B32BP/J-10		TC55B32BP/J-12		TC55B32BP/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	-	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	7	-	8	-	9	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{AW}	Address Valid to End of Write	7	-	8	-	9	-	
t_{WP}	Write Pulse Width	6	-	7	-	8	-	
t_{WR}	Write Recovery Time	1	-	1	-	1	-	
t_{OS}	Data Set Up Time	6	-	7	-	8	-	
t_{OH}	Data Hold Time	0	-	0	-	0	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	5	-	6	-	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

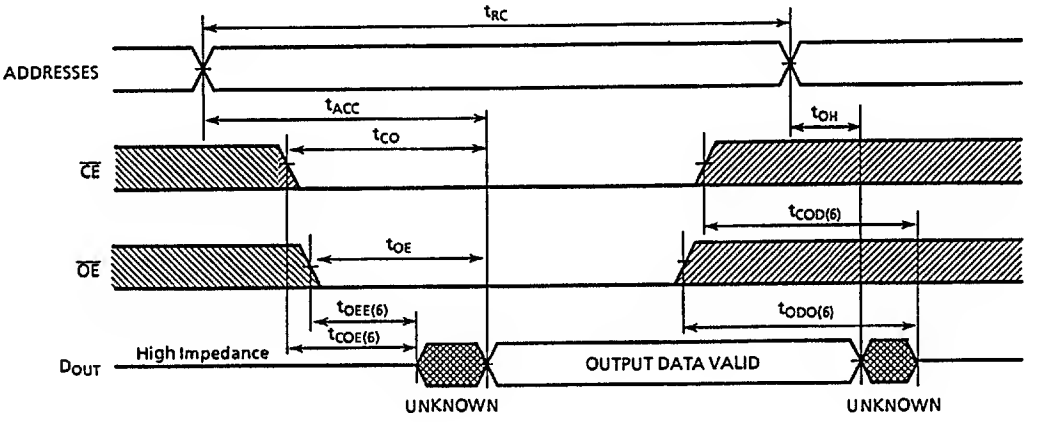
Fig.1



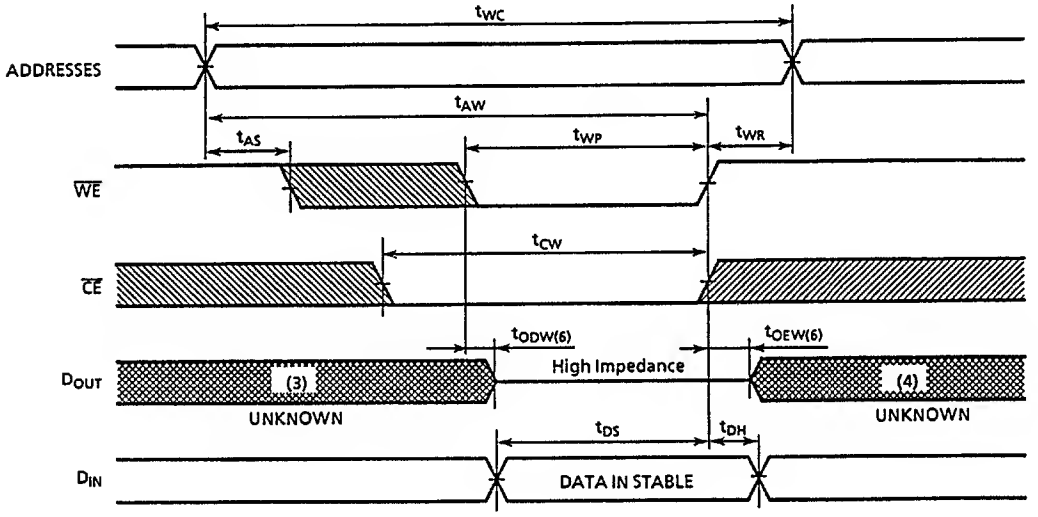
(For t_{COE}, t_{OEE}, t_{COD}, t_{OOO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

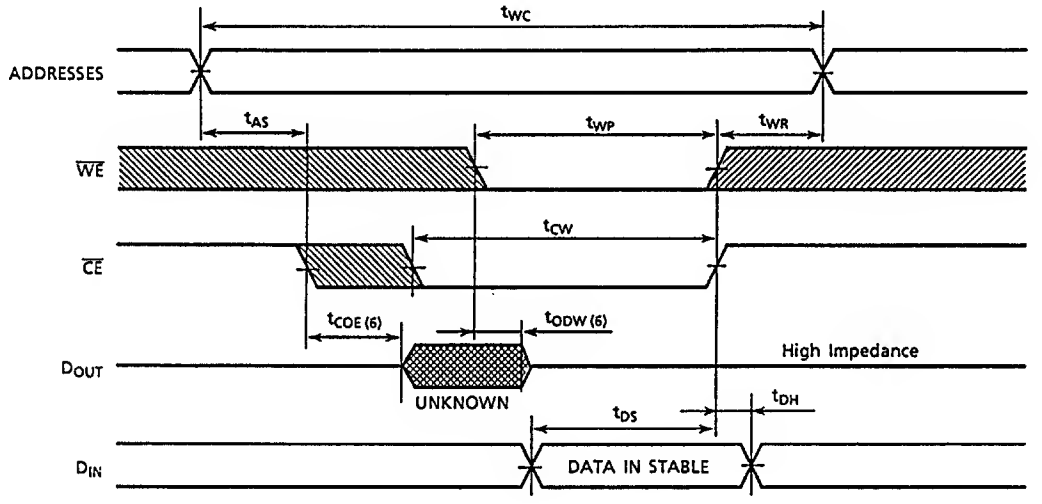
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

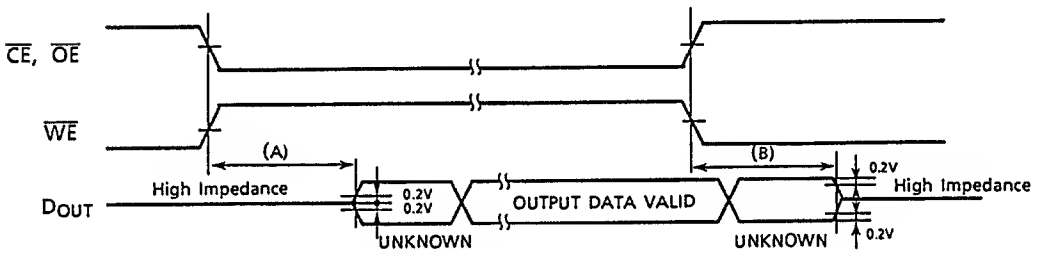
4 Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

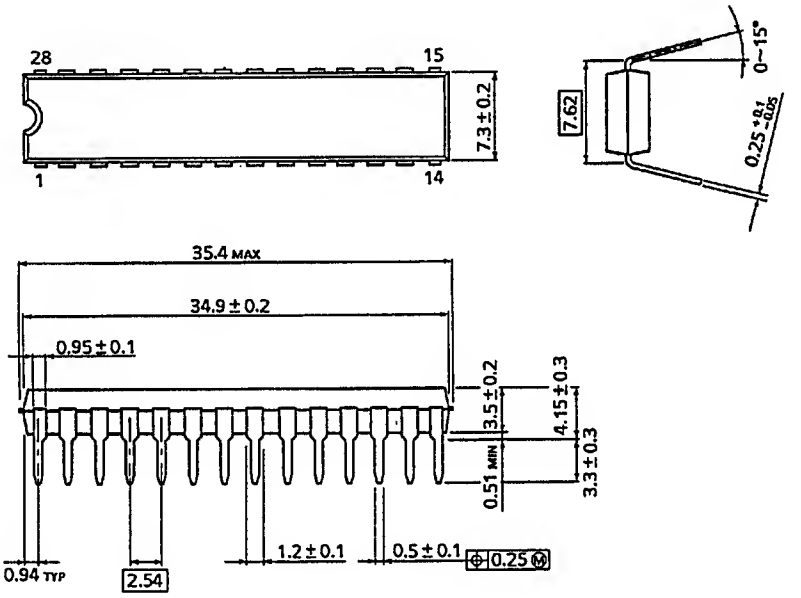
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28 − P − 300B)

UNIT in mm

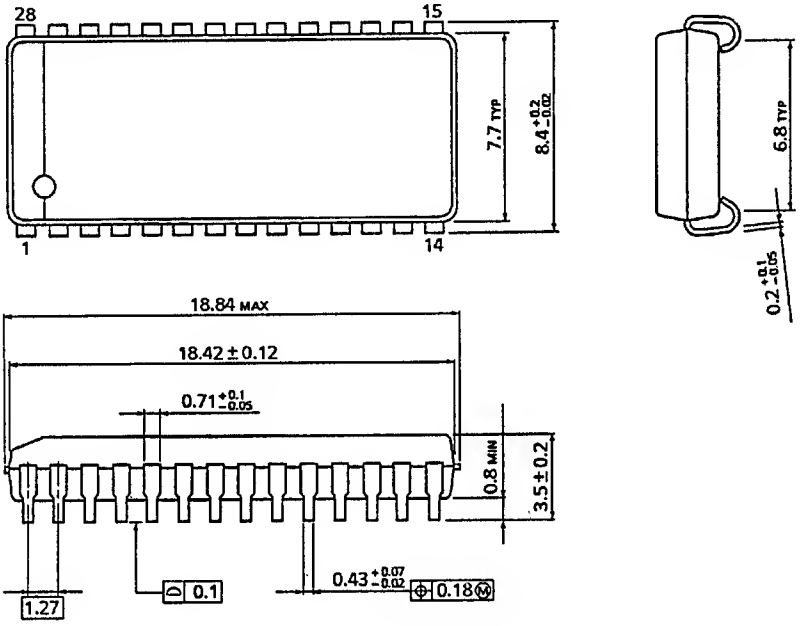


WEIGHT : 2.03g (Typ.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ28 – P – 300A)

UNIT in mm



WEIGHT : 0.83g (Typ.)

32,768 WORD × 9 BIT BiCMOS STATIC RAM PRELIMINARY

DESCRIPTION

The TC55B329P/J is a 294,912 bits high speed static random access memory organized as 32,768 words by 9 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provides high speed feature.

The TC55B329P/J has low power feature with device control using Chip Enable ($\overline{CE1}$/CE2), and has Output Enable Input ($\overline{OE}$) for fast memory access.

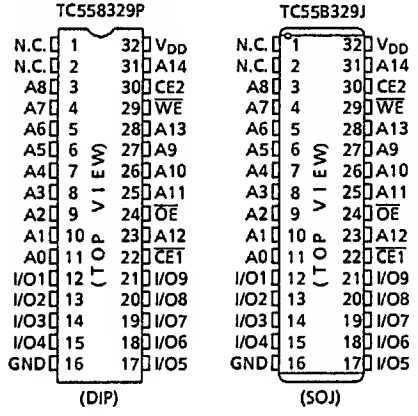
The TC55B329P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B329P/J is packaged in a 32 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B329P/J-10 10ns (MAX.)
  - TC55B329P/J-12 12ns (MAX.)
  - TC55B329P/J-15 15ns (MAX.)
- Low power dissipation
  - Operation : TC55B329P/J-10 170mA (MAX.)
  - TC55B329P/J-12 170mA (MAX.)
  - TC55B329P/J-15 170mA (MAX.)
  - Standby : 15mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55B329P : DIP32-P-300
  - TC55B329J : SOJ32-P-300

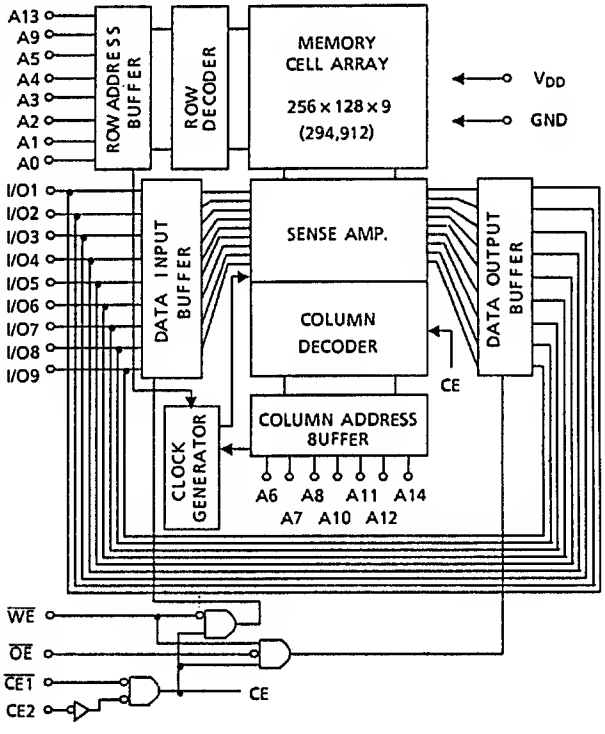
PIN CONNECTION



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	-10~85	°C

* : -3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : -3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL}, Iout = 0mA	-	-	170	mA
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH} or V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	15	

CAPACITANCE (Ta = 25°C, f = 1.0MHZ)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O1~I/O9	POWER
Read	L	H	L	H	Output	I_{DDO}
Write	L	H	*	L	Input	I_{DDO}
Output Disable	L	H	H	H	High Impedance	I_{DDO}
Standby	H	*	*	*	High Impedance	I_{OOS}
	*	L	*	*	High Impedance	I_{DDS}

* : H or L

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B329P/J-10		TC55B329P/J-12		TC55B329P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	-	12	-	15	-	ns
t_{ACC}	Address Access Time	-	10	-	12	-	15	
t_{CO1}	$\overline{CE1}$ Access Time	-	10	-	12	-	15	
t_{CO2}	CE2 Access Time	-	10	-	12	-	15	
t_{OE}	$\overline{OE}$ Access Time	-	5	-	6	-	8	
t_{OH}	Output Data Hold Time from Address Change	3	-	3	-	3	-	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	3	-	3	-	3	-	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	-	5	-	6	-	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	-	1	-	1	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	5	-	6	-	6	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	10	-	12	-	15	

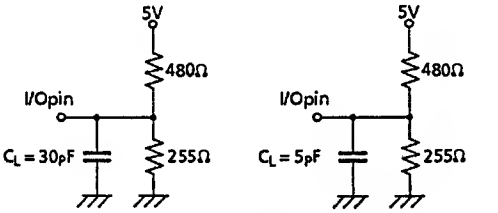
WRITE CYCLE

SYMBOL	PARAMETER	TC55B329P/J-10		TC55B329P/J-12		TC55B329P/J-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	-	12	-	15	-	ns
t_{CW}	Chip Enable to End of Write	7	-	8	-	9	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{AW}	Address valid to end of write	7	-	8	-	9	-	
t_{WP}	Write Pulse Width	6	-	7	-	8	-	
t_{WR}	Write Recovery Time	1	-	1	-	1	-	
t_{DS}	Data Set Up Time	6	-	7	-	8	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	5	-	6	-	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig.1

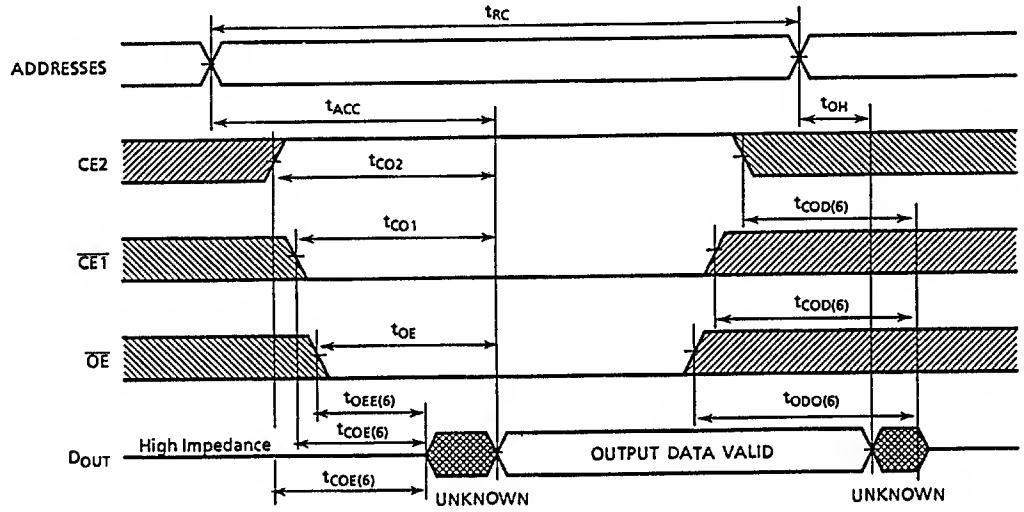
Fig.1



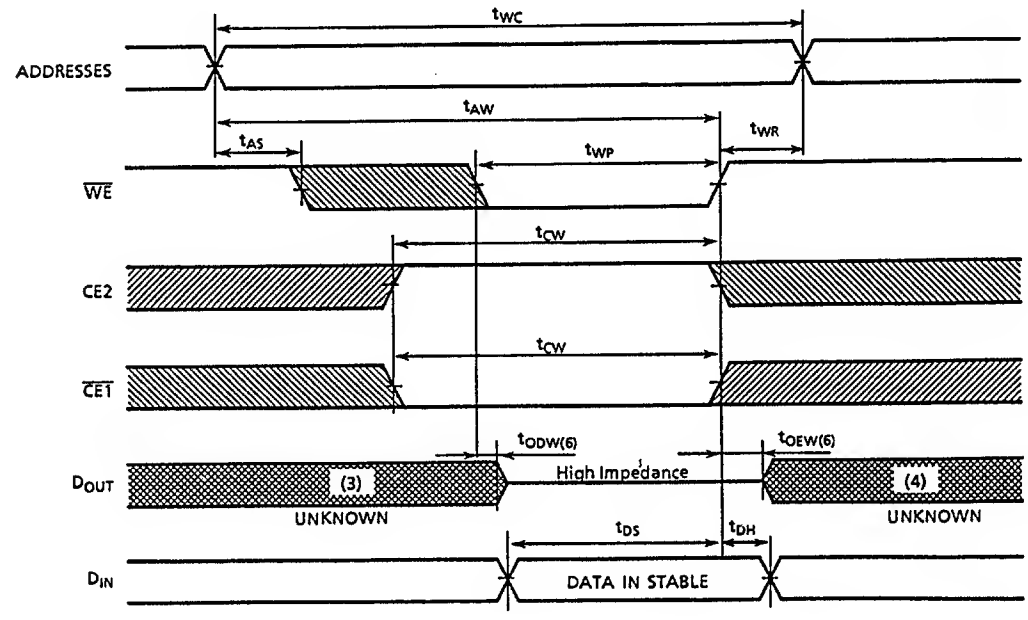
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

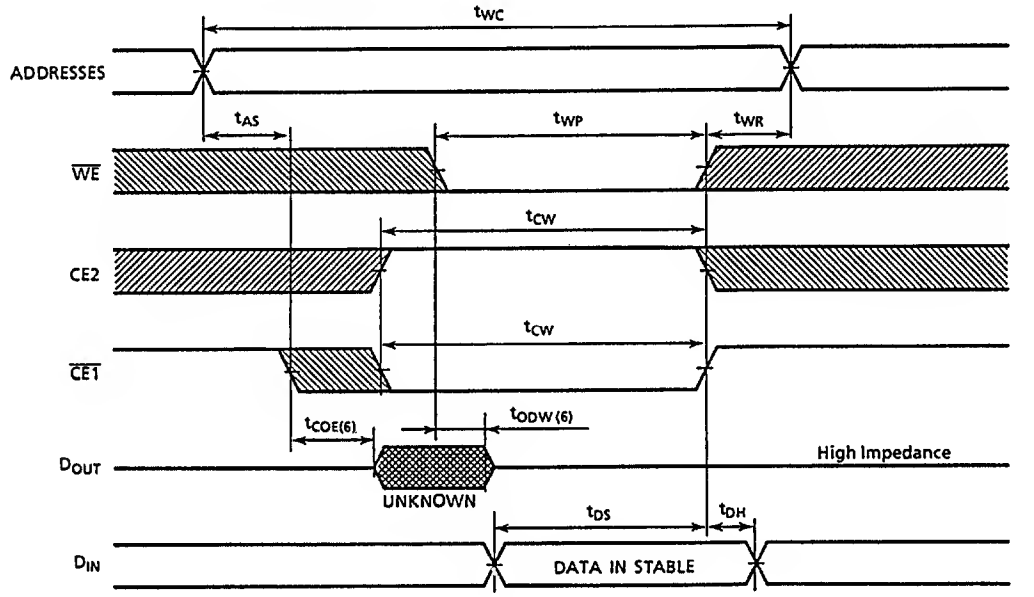
READ CYCLE (2)



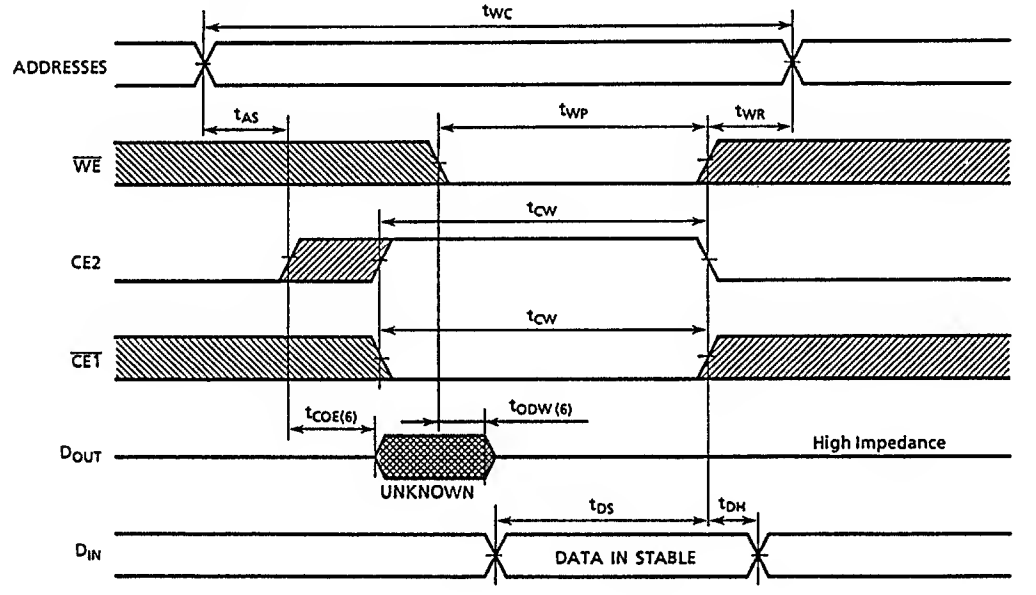
WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

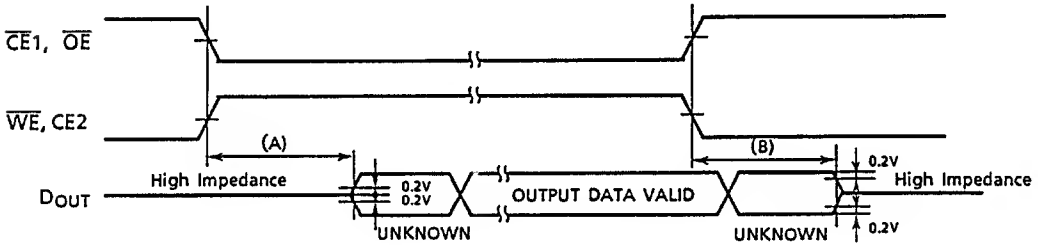
4 Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

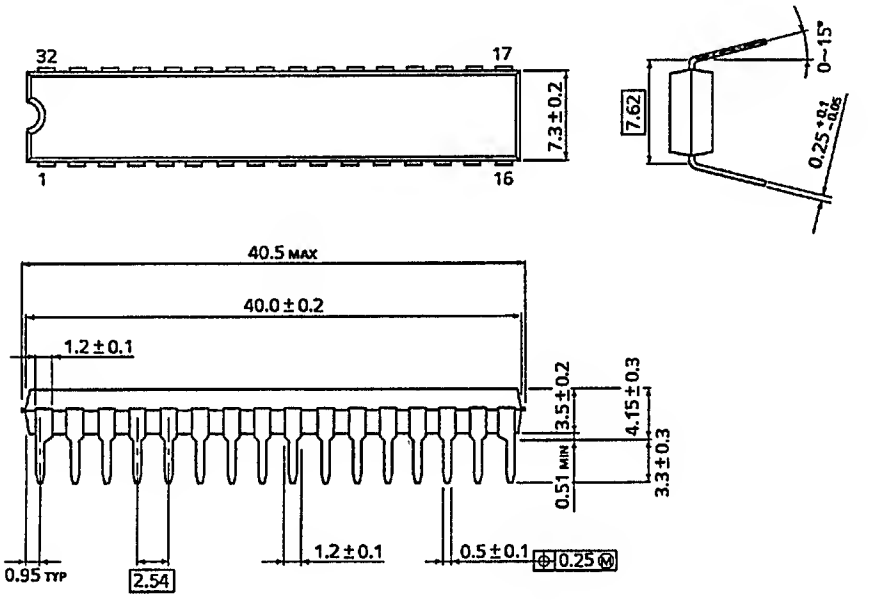
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP32-P-300)

UNIT in mm

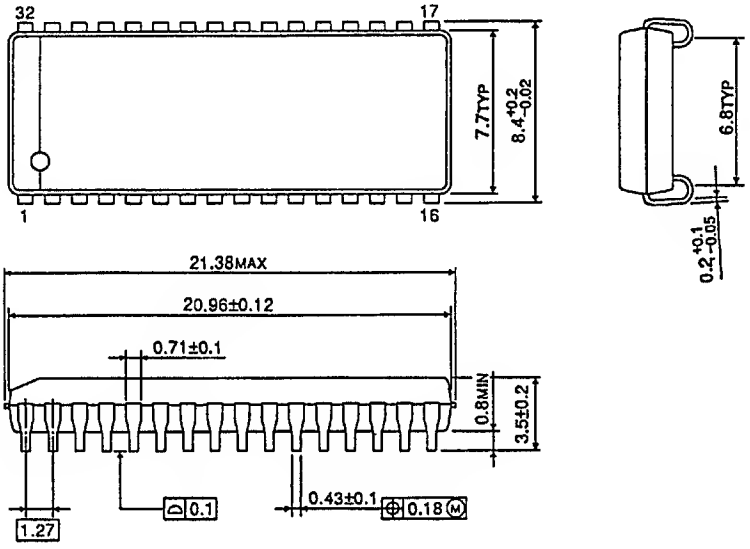


WEIGHT : g (TYP.)

OUTLINE DRAWINGS

Plastic SOJ (SOJ32 − P − 300)

UNIT in mm



WEIGHT : 0.90g (TYP.)

262,144 WORD × 4 BIT BiCMOS STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55B4256P/J is a 1,048,576 bits high speed static random access memory organized as 262,144 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provide high speed feature.

The TC55B4256P/J has low power feature with device control using Chip Enable ($\overline{CE}$).

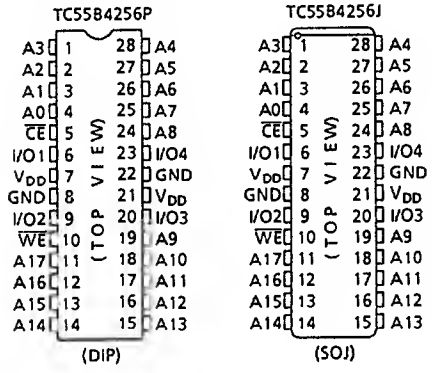
The TC55B4256P/J is suitable for use in various application systems where high speed is required as cache memory, high speed storage, main memory, and so on. All Inputs and Outputs are directly TTL compatible.

The TC55B4256P/J is packaged in a 28 pin standard DIP and SOJ with 400 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B4256P/J-12 12ns (MAX.)
  - TC55B4256P/J-15 15ns (MAX.)
  - TC55B4256P/J-20 20ns (MAX.)
- Low power dissipation
  - Operation : TC55B4256P/J-12 130mA (MAX.)
  - TC55B4256P/J-15 130mA (MAX.)
  - TC55B4256P/J-20 130mA (MAX.)
  - Standby : 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package
  - TC55B4256P : DIP28-P-400A
  - TC55B4256J : SOJ28-P-400

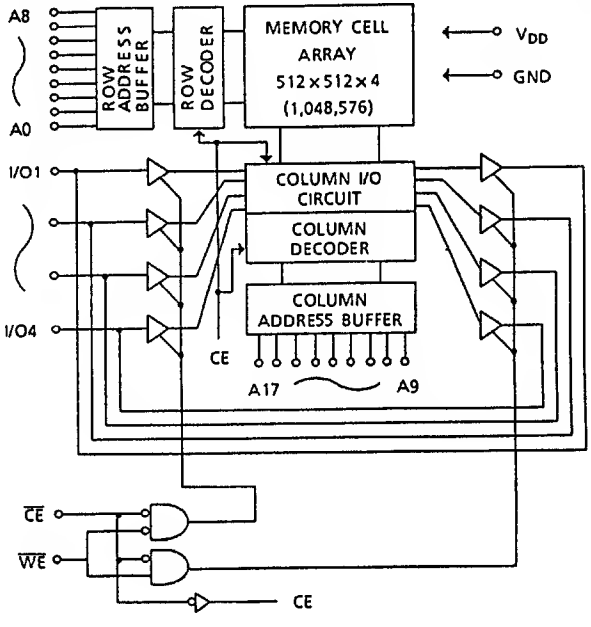
PIN CONNECTION



PIN NAMES

A0~A17	Address Inputs
I/O1~I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0*~7.0	V
$V_{I/O}$	I/O Terminal Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	900	mW
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

* : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH}/V_{IL}	-	-	130	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I/O	POWER
Read	L	H	Dout	I_{DDO}
Write	L	L	Din	I_{DDO}
Standby	H	*	High - Z	I_{DDS}

* High or Low

AC CHARACTERISTICS (Ta = 0~70°C [4], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B4256P/J-12		TC55B4256P/J-15		TC55B4256P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	-	15	-	20	-	ns
t_{ACC}	Address Access Time	-	12	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	12	-	15	-	20	
t_{COE}	Output Enable Time from $\overline{CE}$	4	-	4	-	4	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	6	-	7	-	8	
t_{OH}	Output Data Hold Time from Address Change	4	-	4	-	4	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	12	-	15	-	20	

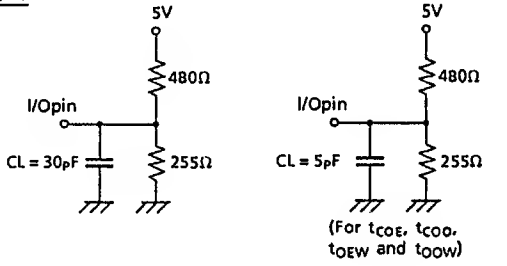
WRITE CYCLE

SYMBOL	PARAMETER	TC55B4256P/J-12		TC55B4256P/J-15		TC55B4256P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	-	15	-	20	-	ns
t_{WP}	Write Pulse Width	8	-	9	-	10	-	
t_{AW}	Address Valid to End of Write	9	-	10	-	11	-	
t_{CW}	Chip Enable to End of Write	8	-	9	-	10	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	1	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	6	-	7	-	8	
t_{DS}	Data Set Up Time	7	-	8	-	9	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

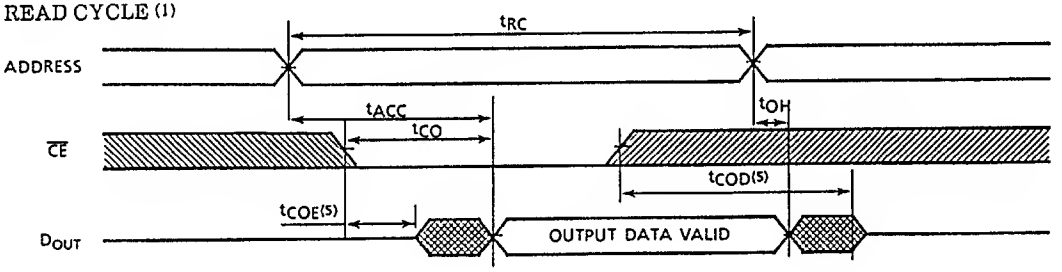
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

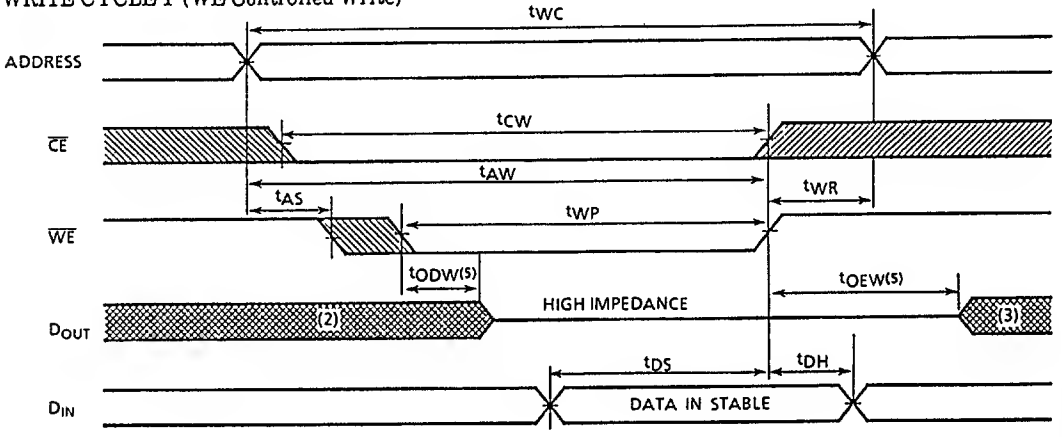


TIMING WAVEFORMS

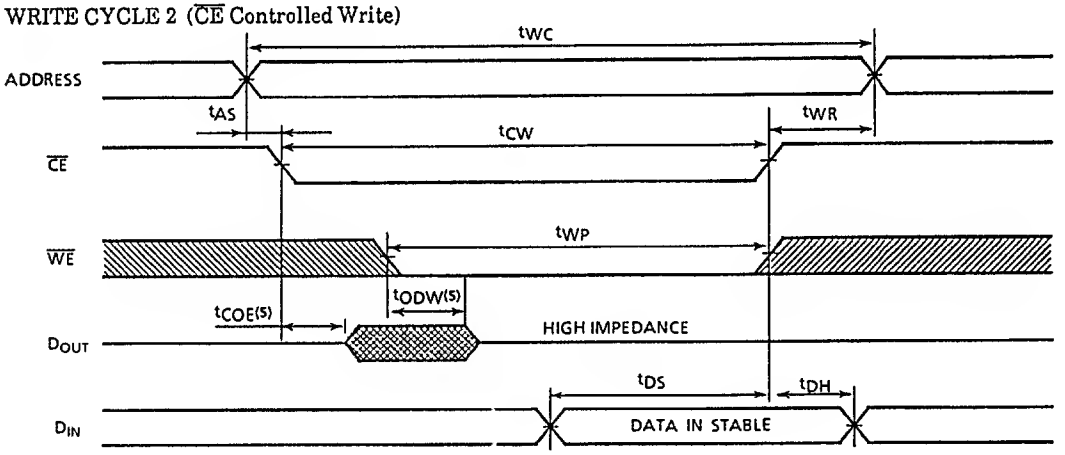
READ CYCLE (1)



WRITE CYCLE 1 (WE Controlled Write)



WRITE CYCLE 2 (CE Controlled Write)



Note :

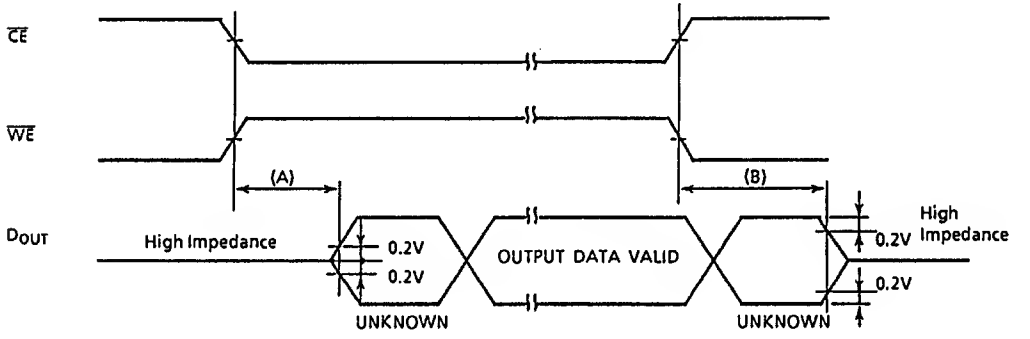
1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

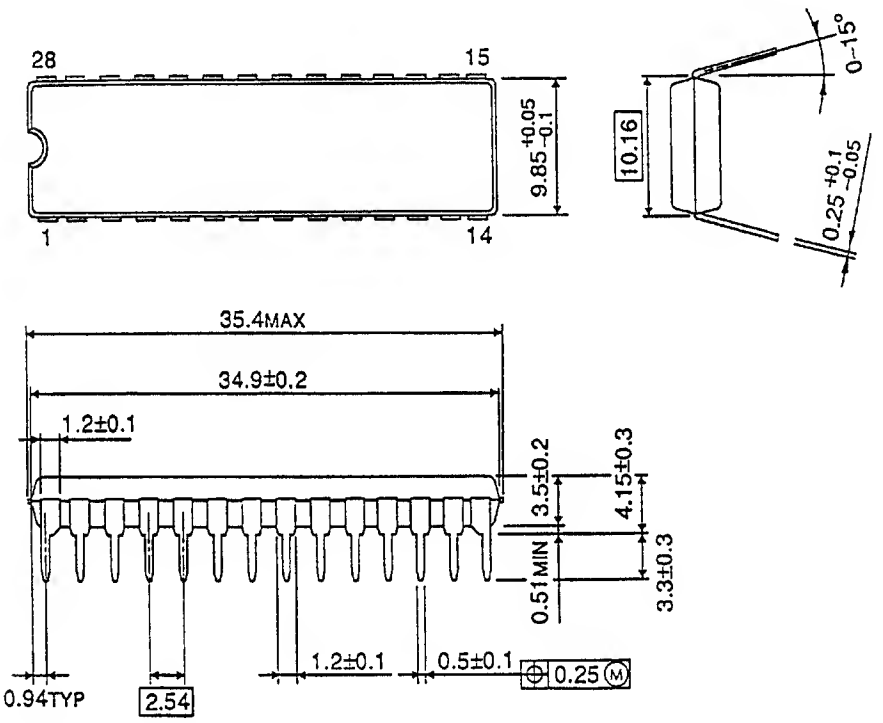
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEW} ..... Output Enable Time
   (B) t_{COD}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28−P−400A)

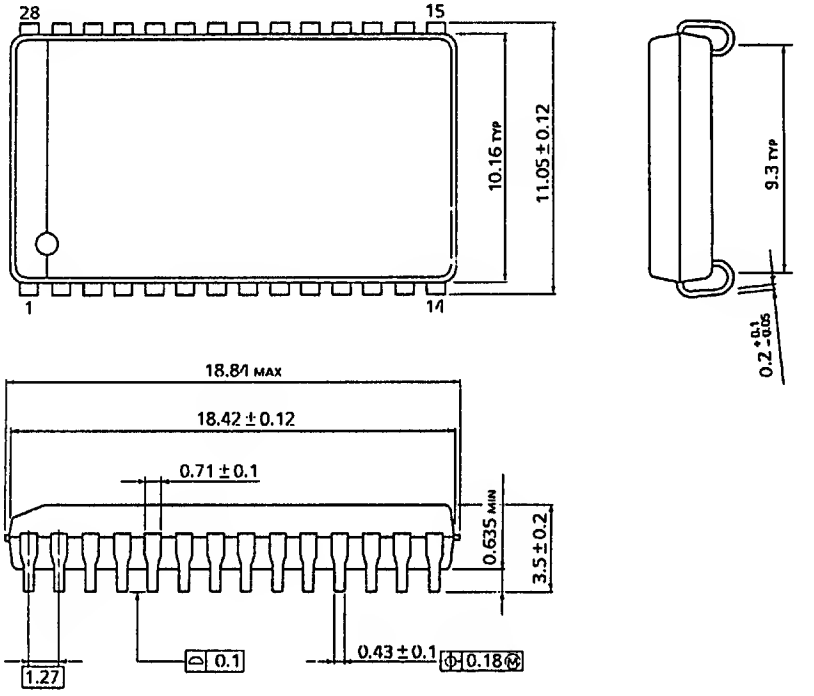
Unit in mm



OUTLINE DRAWINGS

Plastic SOJ (SOJ28−P−400)

Unit in mm



262,144 WORD × 4 BIT BiCMOS STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55B4257P/J is a 1,048,576 bits high speed static random access memory organized as 262,144 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provide high speed feature.

The TC55B4257P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access.

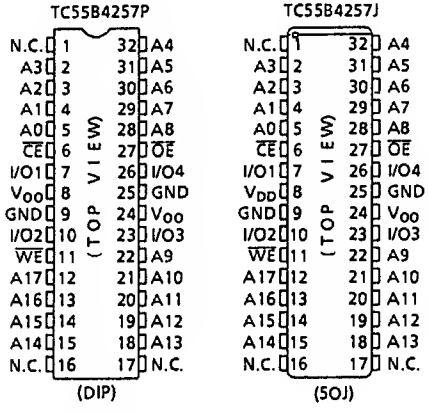
The TC55B4257P/J is suitable for use in various application systems where high speed is required as cache memory, high speed storage, main memory, and so on. All Inputs and Outputs are directly TTL compatible.

The TC55B4257P/J is packaged in a 32 pin standard DIP and SOJ with 400 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B4257P/J-12 12ns (MAX.)
  - TC55B4257P/J-15 15ns (MAX.)
  - TC55B4257P/J-20 20ns (MAX.)
- Low power dissipation
  - Operation : TC55B4257P/J-12 130mA (MAX.)
  - TC55B4257P/J-15 130mA (MAX.)
  - TC55B4257P/J-20 130mA (MAX.)
  - Standby : 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55B4257P : DIP32-P-400
  - TC55B4257J : SOJ32-P-400A

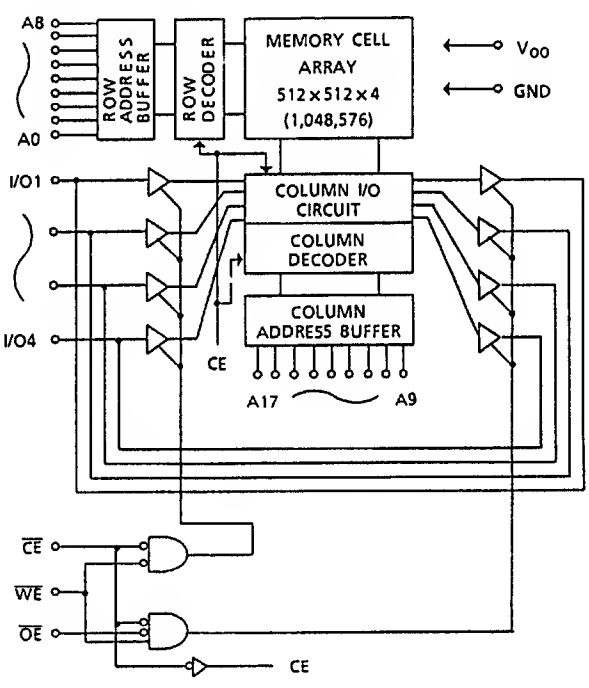
PIN CONNECTION



PIN NAMES

A0~A17	Address Inputs
I/O1~I/O4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0*~7.0	V
$V_{I/O}$	I/O Terminal Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	900	mW
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

*: −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

*: −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH}/V_{IL}	-	-	130	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH}/V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
Read	L	L	H	Dout	I_{DDO}
Write	L	*	L	Din	I_{DDO}
Output Disabled	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* High or Low

AC CHARACTERISTICS (Ta = 0~70°C [4], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B4257P/J - 12		TC55B4257P/J - 15		TC55B4257P/J - 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	-	15	-	20	-	ns
t_{ACC}	Address Access Time	-	12	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	12	-	15	-	20	
t_{OE}	Output Enable Access Time	-	7	-	8	-	10	
t_{COE}	Output Enable Time from $\overline{CE}$	4	-	4	-	4	-	
t_{COO}	Output Disable Time from $\overline{CE}$	-	6	-	7	-	8	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OOO}	Output Disable Time from $\overline{OE}$	-	5	-	6	-	7	
t_{OH}	Output Data Hold Time from Address Change	4	-	4	-	4	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PO}	Chip Deselection to Power Down Time	-	12	-	15	-	20	

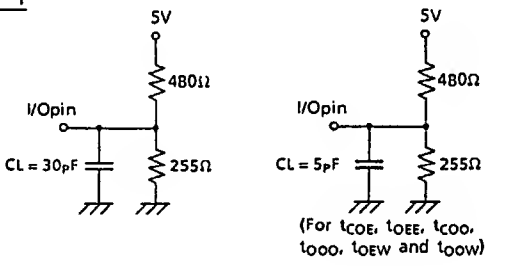
WRITE CYCLE

SYMBOL	PARAMETER	TC55B4257P/J - 12		TC55B4257P/J - 15		TC55B4257P/J - 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	-	15	-	20	-	ns
t_{WP}	Write Pulse Width	8	-	9	-	10	-	
t_{AW}	Address Valid to End of Write	9	-	10	-	11	-	
t_{CW}	Chip Enable to End of Write	8	-	9	-	10	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	1		
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{OOW}	Output Disable Time from $\overline{WE}$	-	6	-	7	-	8	
t_{OS}	Data Set Up Time	7	-	8	-	9	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

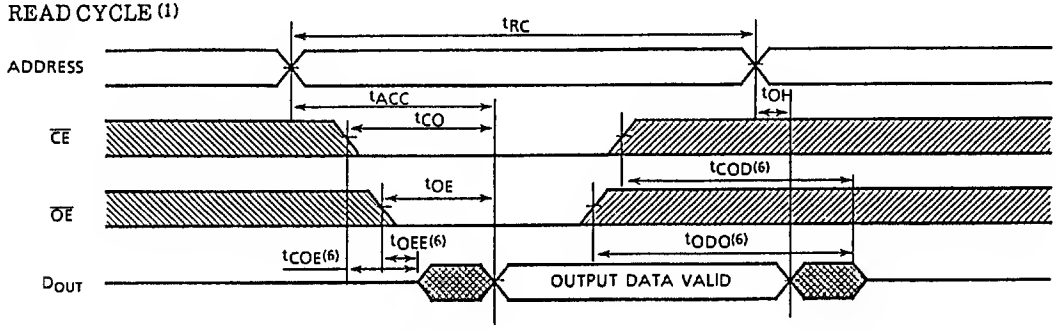
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

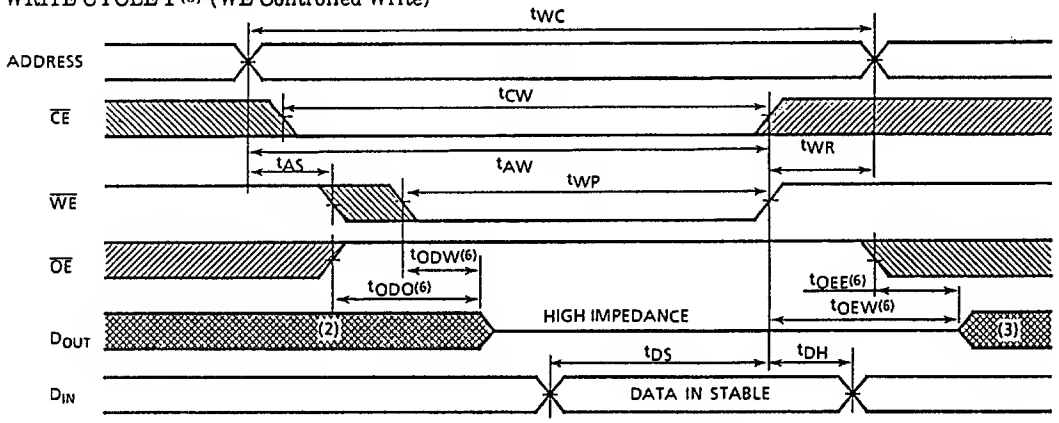


TIMING WAVEFORMS

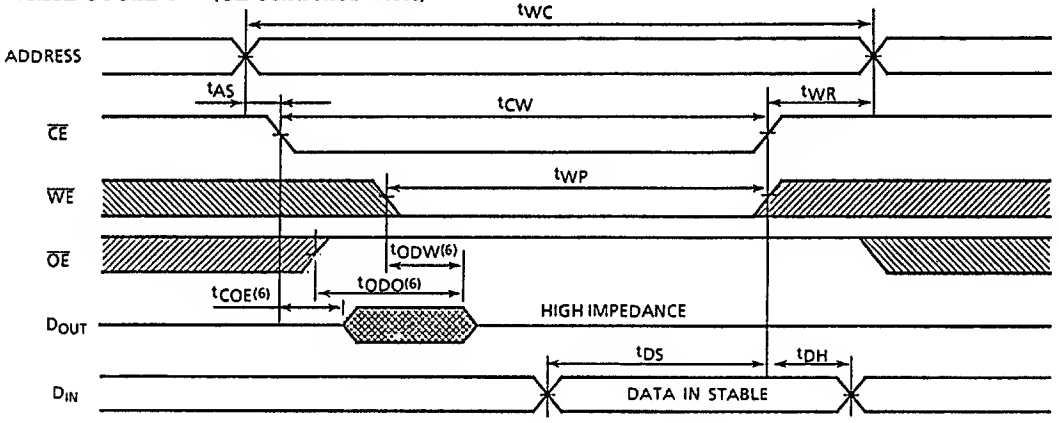
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.

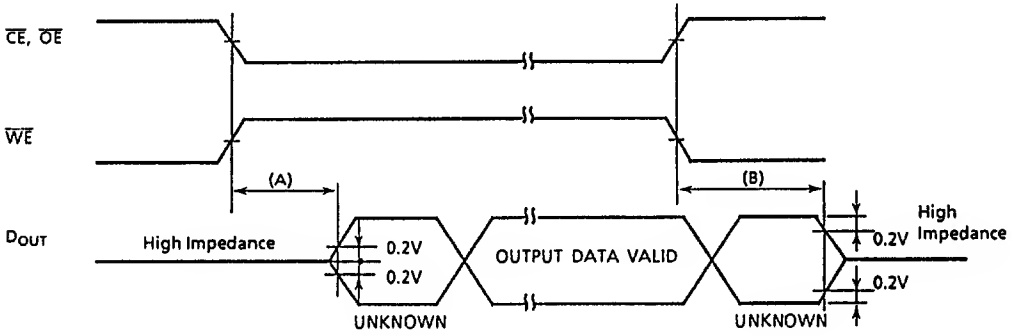
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

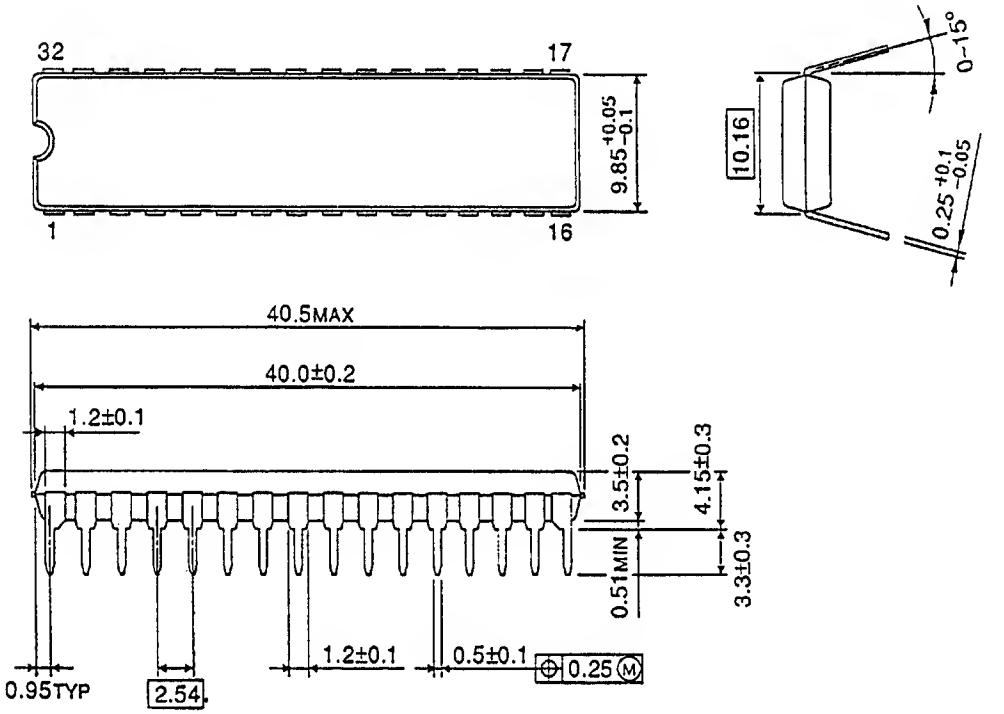
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP32−P−400)

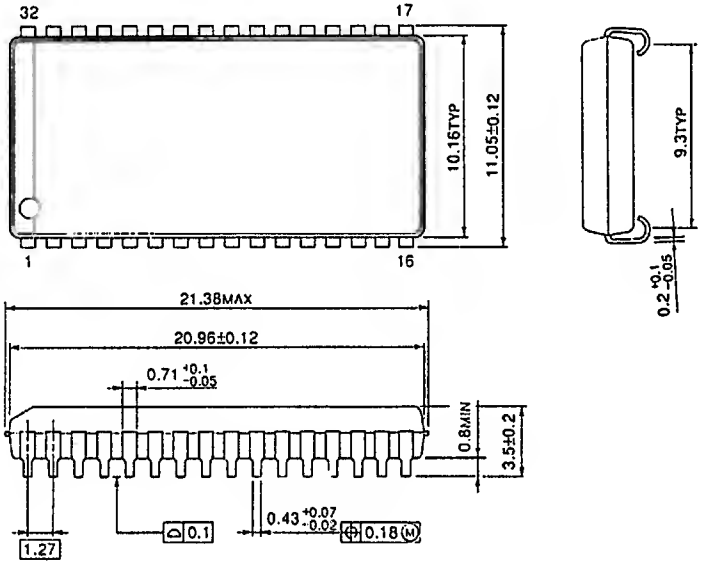
Unit in mm



OUTLINE DRAWINGS

Plastic SOJ (SOJ32−P−400A)

Unit in mm



131,072 WORD × 8 BIT BiCMOS STATIC RAM PRELIMINARY

DESCRIPTION

The TC55B8128P/J is a 1,048,576 bits high speed static random access memory organized as 131,072 words by 8 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provide high speed feature.

The TC55B8128P/J has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable Input ($\overline{OE}$) for fast memory access.

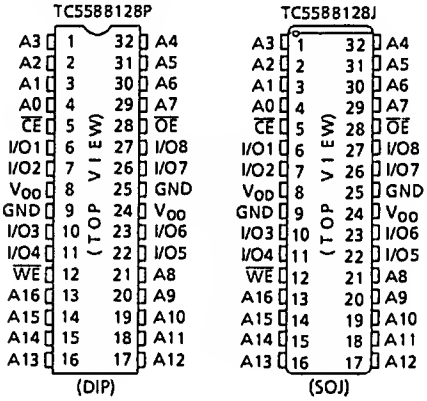
The TC55B8128P/J is suitable for use in cache memory where high speed is required. All Inputs and Outputs are directly TTL compatible.

The TC55B8128P/J is packaged in a 32 pin standard DIP and SOJ with 400 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B8128P/J-12 12ns (MAX.)
  - TC55B8128P/J-15 15ns (MAX.)
  - TC55B8128P/J-20 20ns (MAX.)
- Low power dissipation
  - Operation : TC55B8128P/J-12 150mA (MAX.)
  - TC55B8128P/J-15 150mA (MAX.)
  - TC55B8128P/J-20 150mA (MAX.)
  - Standby : 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - TC55B8128P : DIP32-P-400
  - TC55B8128J : SOJ32-P-400A

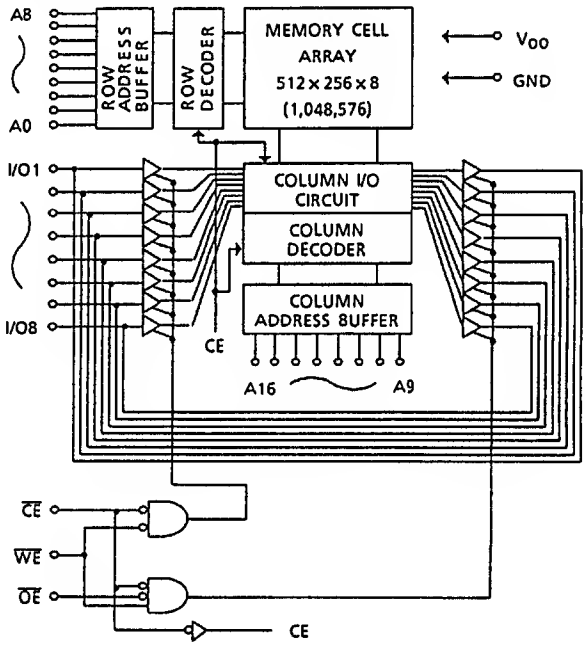
PIN CONNECTION



PIN NAMES

A0~A16	Address Inputs
I/O1~I/O8	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0*~7.0	V
$V_{I/O}$	I/O Terminal Voltage	-0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	900	mW
Tsolder	Soldering Temperature·Time	260·10	°C·sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

*: −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

*: −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH}/V_{IL}	-	-	150	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH}/V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
Read	L	L	H	Dout	I_{DDO}
Write	L	*	L	Din	I_{DDO}
Output Disabled	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* High or Low

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ [4], $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	-	15	-	20	-	ns
t_{ACC}	Address Access Time	-	12	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	12	-	15	-	20	
t_{OE}	Output Enable Access Time	-	7	-	8	-	10	
t_{COE}	Output Enable Time from $\overline{CE}$	4	-	4	-	4	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	6	-	7	-	8	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	5	-	6	-	7	
t_{OH}	Output Data Hold Time from Address Change	4	-	4	-	4	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	12	-	15	-	20	

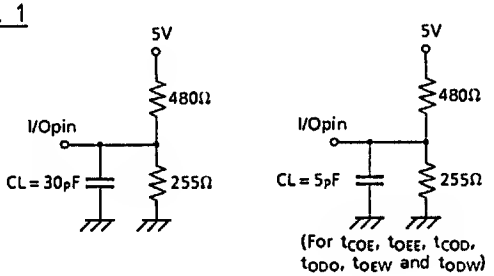
WRITE CYCLE

SYMBOL	PARAMETER	TC55B8128P/J-12		TC55B8128P/J-15		TC55B8128P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	-	15	-	20	-	ns
t_{WP}	Write Pulse Width	8	-	9	-	10	-	
t_{AW}	Address Valid to End of Write	9	-	10	-	11	-	
t_{CW}	Chip Enable to End of Write	8	-	9	-	10	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	1		
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	6	-	7	-	8	
t_{DS}	Data Set Up Time	7	-	8	-	9	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

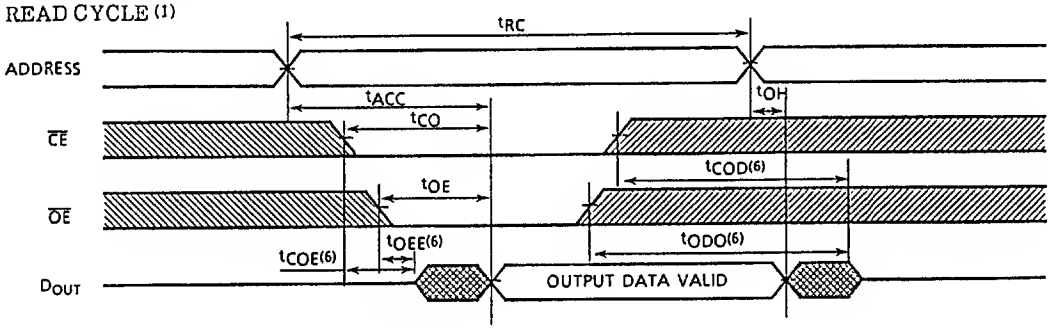
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

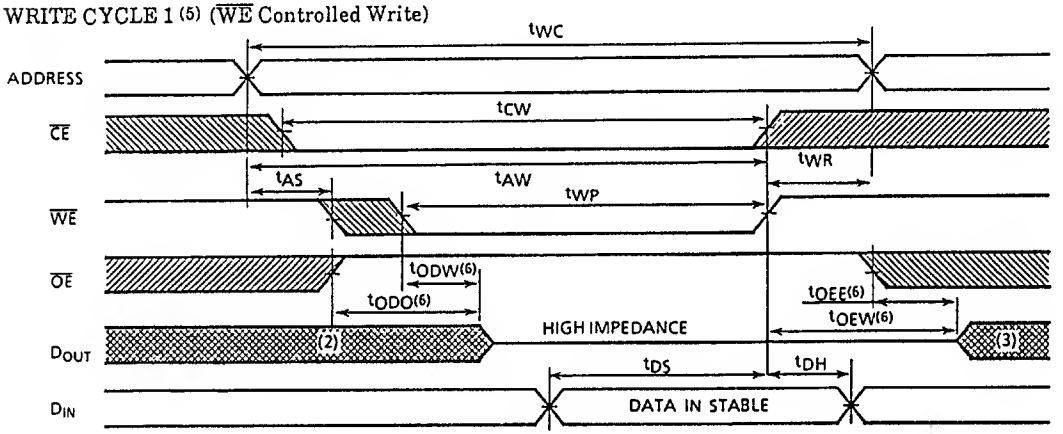


TIMING WAVEFORMS

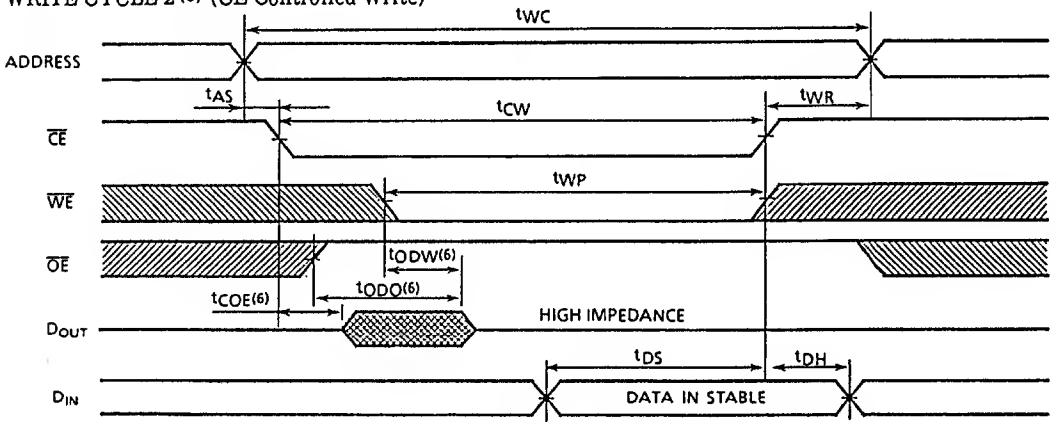
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)

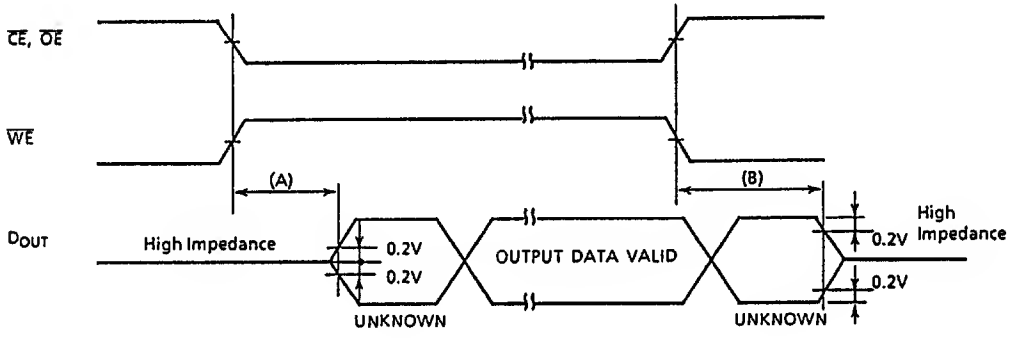


WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note :

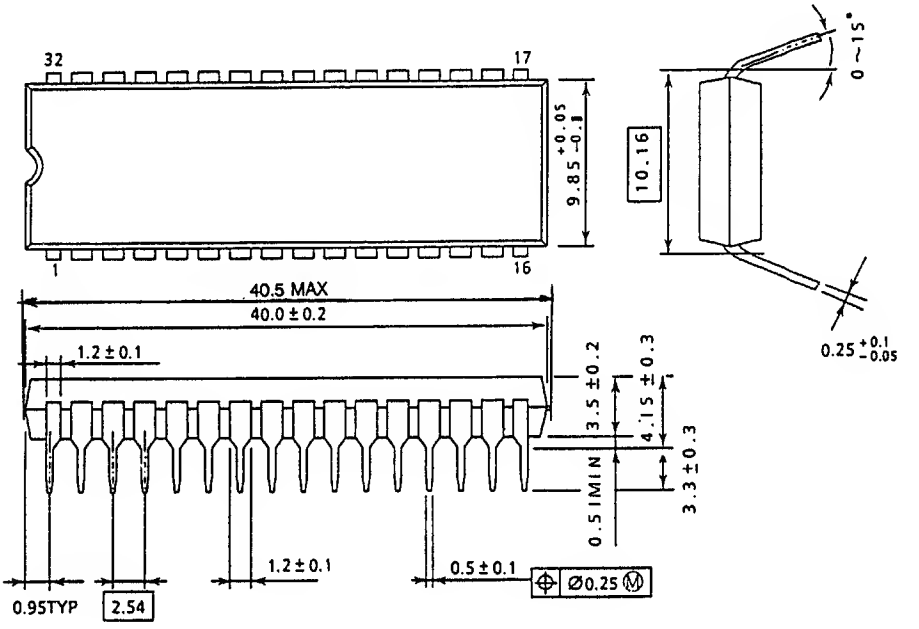
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP32−P−400)

Unit in mm

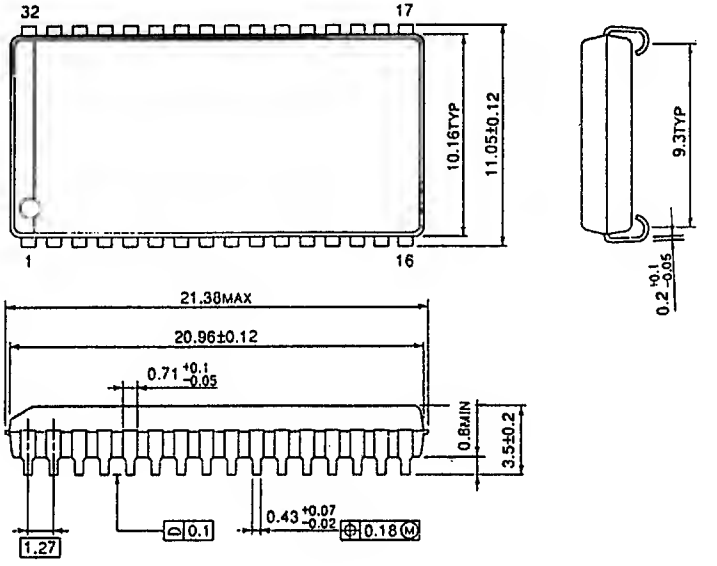


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ32−P−400A)

Unit in mm



TAEC SALES OFFICES

NORTHWEST AREA
490-B Lakeside Drive
Sunnyvale, CA 94086
TEL: (408) 737-9844
FAX: (408) 737-9905

PACIFIC NORTHWEST DISTRICT
1700 N.W. 167th Place, Suite 240
Beaverton, OR 97006
TEL: (503) 629-0818
FAX: (503) 629-0827

SOUTHWEST AREA
15621 Redhill Avenue, Suite 205
Tustin, CA 92680
TEL: (714) 259-0368
FAX: (714) 259-9439

NORTH CENTRAL REGION
One Parkway North, Suite 500
Deerfield, IL 60015-2547
TEL: (708) 945-1500
FAX: (708) 945-1044

SOUTH CENTRAL REGION
777 E. Campbell Road, Suite 650
Richardson, TX 75081
TEL: (214) 480-0470
FAX: (214) 235-4114

NORTHEAST AREA
25 Mall Road, 5th Floor
Burlington, MA 01803
TEL: (617) 272-4352
FAX: (617) 272-3089

NORTHEAST REGION (MID-ATLAN
303 Lippincott Center, Suite 120
Marlton, NJ 08053
TEL: (609) 985-3737
FAX: (609) 985-6814

SOUTHEAST AREA
Waterford Centre
5555 Triangle Parkway, Suite 300
Norcross, GA 30092
TEL: (404) 368-0203
FAX: (404) 368-0075

SOUTHEAST REGION
600 S. North Lake Blvd., Suite 250
Altamonte Springs, FL 32701
TEL: (407) 332-0966
FAX: (407) 339-3777

SOUTHEAST DISTRICT
5511 Capitol Center Drive, Suite 308
Raleigh, NC 27606
TEL: (919) 859-2800
FAX: (919) 859-2898

TOSHIBA

MST-0101/3-92